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AN ILS APPROACH PROGRAMME UNIT FOR THE RADIO ENVIRONMENT MONITOR

by

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SUMMARY

A programme unit is described which is capable of providing appropriate voltage levels into a signal simulator which in turn supplies the necessary RF signal input to the radio environment monitor in such a way as to simulate an ILS approach by an aircraft.

The approach can be simulated with or without the various forms of interference which the monitor is capable of detecting.

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CONTENTS

1 INTRODUCTION

During the early development stages of the ILS (Instrument Landing System) radio environment monitor[1], it became necessary to simulate the type of signal environment in which the monitor had to operate. The monitor operates basically from three input signals. The first is the signal received directly from the ILS transmitter being monitored, to the carrier of which the monitor is phase locked. The second signal channel is derived from a high gain aerial array beamed on the approaching aircraft so that the Doppler shifted reflection of the transmitted ILS signals is received. Superimposed on this channel will be any re-radiated ILS signals and externally generated (rogue) interference signals received by the aircraft. These interference signals are also Doppler shifted relative to the transmitter carrier frequency. The third input consists of 75 MHz modulated signals reflected back to the monitor from the aircraft as it passes over each marker beacon on the approach.

A special-to-type signal generator was therefore developed to reproduce this type of signal environment and is known as the signal simulator.

The signal simulator was designed in such a manner that the variation of the parameters of frequency and amplitude were obtained mainly by means of voltage control. The necessary control lines were made available at a socket via a remote/local switch so that the simulator could be operated from an external source.

Advantage was taken of this external control to design a programme unit which would operate the signal simulator in such a manner as to reproduce the order of signals received from an aircraft during an approach over approximately 5 miles to touchdown. It was also required to generate the various forms of interference likely to be received by the aircraft at any stage during the approach.

2 THE SIGNAL SIMULATOR

The simulator is designed in three sections, namely localiser, glide path and marker sections.

The glide path section is dependent upon the localiser section in that is uses the same drive circuits.

The localiser (Fig.1) and glide path sections each provide a reference output which can be pre-set to the channel in use and modulated with the

appropriate DDM (Difference in Depth of Modulation) at 90 and 150 Hz. No external control is required on these outputs other than a facility for modulating the localiser signals with an external identification and timing audio frequency.

The two sections also have a second channel each which simulates the reflected signal. Both the signal frequency and amplitude of these channels can be varied externally.

There are also facilities for switching into this second channel, re-radiated and/or rogue interference signals, the frequency and amplitudes of which can also be varied externally.

The marker section (Fig.2) generates a modulated output on 75 MHz which can be switched on externally, and also controlled with respect to the coded modulation frequency corresponding to the particular marker beacon required.

A more detailed description of the operation of the signal simulator is given in Appendix A.

3 THE PROGRAMME UNIT

The programme unit is designed around the approach layout and order of signals which have been measured at Heathrow, London Airport on runway 28 left (28L).

A simplified block diagram of the composition of the unit is shown in Fig.3

3.1 Normal approach programme

The basic drive for the programme unit is a circuit called the approach time ramp generator. This consists of a linear integrator which derives its input from the voltage across a potentiometer calibrated from 120 to 160 knots. The potentiometer is set to the required mean aircraft approach speed and the ramp generator adjusted to integrate over a time proportional to the distance to be travelled, i.e. from just before the outer marker overfly to just after passing the monitor directional aerial.

The output from the ramp generator is connected to three identical marker range gates. These gates can be set to operate at any point along the ramp to give a pulse duration of any width. They can therefore be set up to reproduce the time duration of the reflected marker pulses normally received by the monitor. The three output pulses are connected to the signal simulator to operate the relevant marker tone gates.

The diagram shown in Fig.4 illustrates the distances and running times involved over the 28L approach path.

The voltage across the approach speed potentiometer is connected to the signal simulator through a speed/simulator interface circuit. This circuit transposes the voltage to the value and polarity required to off-set the reflected signal output frequency by the radar Doppler shift corresponding to the speed setting.

The output of the approach time ramp generator is connected to a second integrator known as the approach field strength curve generator. This circuit can be adjusted to produce a typical type of signal strength curve as measured on runway 28L. The integrator is allowed to limit just before the middle marker position is reached in order to flatten out the curve. Just after the middle marker is passed, the integrating capacitor is automatically discharged at a different rate in order to reproduce the rapid fall off in signal strength as the aircraft nears runway threshold.

A typical curve as produced by the programme unit is shown in Fig.5. The curve thus produced is fed through interface circuits to the signal simulator voltage controlled attenuators so that the necessary voltage/dB conversion can be adjusted.

In order to produce a variable DDM on both the localiser and glide path reflected signals, the 90 and 150 Hz tones generated within the signal simulator are brought out to the programme unit where they are fed through voltage controlled amplifiers before being mixed and fed back into the signal simulator reflected signal modulator. The gain of the voltage controlled amplifiers is varied differentially from a circuit which produces a very low frequency sinewave of decreasing amplitude to simulate the type of approach an aircraft might make in beam joining and lining up. An example of the control curve is shown in Fig.6.

In order to complete the normal approach programme so far produced, coded runway 28L identification signals at 1020 Hz and coded timing signals at 4000 Hz are generated within the programme unit and fed to the carrier modulators in the signal simulator,

3.2 Interference programme

Three types of interferences are generated by the programme unit on demand, namely aircraft overfly interference, fixed frequency interference and sweep frequency interference.

3.2.1 Aircraft overfly interference

This is produced by a linear ramp generator the output voltage from which is fed through an interface circuit to the voltage controlled oscillator in the signal simulator which in turn provides the drive for the re-radiated interference output. The interface circuit is adjusted so that when the re-radiated interference frequency is switched on, the output frequency is identical to the reflected signal frequency. As the ramp voltage rises so the re-radiated interference frequency is slowly pulled away from the reflected signal frequency to simulate the effect of another aircraft overflying the localiser. The time along the approach during which this takes place is determined by a range gate connected to the approach time ramp generator and can therefore be pre-set to operate at any point.

3.2.2 Fixed frequency interference

The point along the approach when this occurs and the time duration is also controlled by a pre-set range gate connected to the approach time ramp generator. The range gate output operates a relay which switches on the rogue frequency interference RF in the signal simulator. It also connects the output of a potentiometer, which is connected across a voltage supply, to the rogue interference voltage controlled oscillator in the signal simulator enabling the interfering frequency to be pre-set.

3.2.3 Sweep frequency interference

The operation of the circuits which provide this form of interference, function in the same way as the fixed frequency interference with the exception that the potentiometer supplying the voltage controlled oscillator in the signal simulator is replaced by a ramp generator which supplies the necessary variable voltage to sweep the frequency across the band.

Both the fixed and sweep frequency interference functions can be selected to operate on either the localiser or glide path outputs of the signal simulator by switching of the appropriate RF relays.

A more detailed description of all the circuits used in the programme unit is given in Appendix B.

4 OPERATION OF PROGRAMME UNIT

Apart from the variable speed setting, the rest of the front panel controls consist of switches (Fig.7). These switches are in the form of illuminated and engraved indicators which when depressed actuate a switch mechanism mounted behind the lamp assembly. Apart from the reset and start

switches which are spring loaded, the rest of the switches are of the push on - push off variety.

The top row of switches and indicators under the heading of aircraft programme are engraved as follows:-

Start approach
Aircraft approaching/aircraft landed
Outer marker on/aircraft overflying
Middle marker on/aircraft overflying
Inner marker on/aircraft overflying
Ident.on/28L/28R
Timing on/code.

The bottom row of switches are under the heading of interference programme and are engraved as follows:-

Reset
Overfly int/aircraft overflying
Spare
Localiser/glide path
Fixed freq int/on
Sweep freq int/on
Spare

After switching on the illuminated push switch engraved mains on, the RESET push switch is operated to set all the circuits.

To set up the approach programme the required number of marker beacons are swtiched on by depressing the push switch to illuminate the top half of the indicator, e.g. OUTER MARKER ON. The required runway code, i.e. 28L or 28R and TIMING ON is selected in the same way so that the appropriate segment of the indicator is illuminated.

To start an approach the start approach switch is depressed momentarily. The IDENT ON indicator will start to flash the selected runway identification coding and the timing CODE indicator will flash a timing code every minute. After a delay (which can be pre-set internally) the AIRCRAFT APPROACHING indicator will illuminate indicating that the signal simulator is producing reflected signals.

When the time period is reached when the aircraft would have flown over a marker, the relevant aircraft overflying indicator will be illuminated, provided that marker has been selected.

At a time corresponding to touchdown the AIRCRAFT APPROACHING indicator will extinguish and the AIRCRAFT LANDED indicator will flash for approximately 5 seconds.

To set up an interference programme the relevant switch is depressed to select whichever interference is required. During the time on the approach when the interference is being generated, the lower half of the indicator on the switch will be automatically illuminated.

The overfly interference is generated only in the localiser section of the signal simulator whereas the fixed and sweep frequency interference can be selected to operate on either the localiser or glide path section by means of the localiser/glide path switch.

Appendix A

SIGNAL SIMULATOR

A.1 The signal simulator

The simulator is designed in three parts, localiser, glide path and marker. The glide path section uses the same drive circuits for producing the reference, reflected and interference signals as the localiser section.

The RF circuit used for the glide path section is similar in design principle to the localiser section the difference being mainly one of frequency.

A.2 The localiser section (Channel 1)

A simplified block diagram of the localiser section is shown in Fig.1. The drive for the transmitter reference signal is obtained from a 10 MHz crystal oscillator. The output from this oscillator is fed into a modulator where it can be modulated by 90 and 150 Hz tone frequencies with a variable DDM. Thus the reference signal can be set up to have the same DDM as seen by the monitor on site. The signal at this point can also be modulated by 1020 Hz or 4000 Hz tone frequencies to simulate identification and timing signals.

From the modulator the signal is fed to the first mixer and amplifier where it is mixed with the output from the first local oscillator. The frequency of this oscillator is determined by a crystal which can be selected to put the final output on the localiser channel frequency required.

The signal is then fed to a second mixer and amplfier where it is mixed with the output from an 85 MHz crystal oscillator which transfers the signal frequency into the localiser band.

The signal is finally connected to an amplifier and attenuator so that the reference output can be set up to be the same level as that seen by the monitor on site.

The circuits so far described are only capable of being operated locally on the simulator as the settings required apertain only to the signal received direct at the monitor from the ILS transmitter and do not vary during the approach. The identification and timing modulator input circuit can however be switched to an external position to accept external generated and coded tone frequencies.

A.3 The localiser section (Channel 2)

The simulated reflected and interference signals which can appear together on the second channel output are produced in the same manner using the same first and second local oscillators as the reference signal channel thereby keeping the frequency drift in each channel the same.

The signals which can be generated are as follows:-

(i) Aircraft reflected signal.

(ii) Re-radiated interference.

(iii) Rogue frequency interference.

Each signal is generated in the same way to produce a drive frequency centred on 10 MHz. The reflected and re-radiated interference signals are each fed through modulators where variable DDM at 90 and 150 Hz, identification and timing signals are added. Provision is made for switching the reflected signal modulator DDM input, to connect in an externally generated and programmed 90/150 Hz signal.

All three signals are fed through independent voltage controlled attenuators so that the signal levels can be varied either locally with potentiometers across a voltage supply or externally by means of a programmed voltage. The control laws for the localiser and glide path sections are shown in Figs.8 and 9 respectively.

To simulate the effect of aerial back-to-front ratio a portion of the Channel 1 signal is fed across to Channel 2 via an attentuator.

A.4 The drive circuits (Channel 2)

The method by which the different drive frequencies are obtained is shown in Fig.10.

A voltage controlled oscillator on 10002 kHz is mixed with the 10 MHz crystal oscillator and the difference frequency compared in a phase sensitive detector with the output from a 2 kHz reference oscillator. The output from the phase sensitive detector controls through a dc amplifier the frequency of the 10002 kHz osciallator in such a manner that a frequency difference of 2 kHz is always maintained with the 10 MHz oscillator irrespective of any drift in this oscillator.

The output of the 10002 kHz oscillator is used as a reference for each of the three frequencies generated on the second channel.

The second half of the block diagram shown in Fig.10 illustrates the circuit which produces the aircraft reflected signal, i.e. the carrier is Doppler shifted in frequency with respect to the transmitter reference signal in Channel 1.

The 10002 kHz oscillator output is connected to a mixer together with the output from a voltage controlled oscillator covering the frequency band 10 MHz ±90 Hz . The difference frequency from the mixer is fed to a phase sensitive detector together with the output from a variable reference oscillator covering the frequency range from 1910 Hz to 2090 Hz. The phase sensitive detector output is connected through a dc amplifier to the 10 MHz ±90 Hz controlled oscillator such that the mixer output is always equal in frequency to the variable reference oscillator.

Thus a drive frequency is produced which will differ in frequency from the 10 MHz transmitter reference drive by an amount equal to the difference in frequency between the variable reference oscillator and the 2 kHz fixed reference oscillator. This frequency is measured and displayed on a meter.

The other two circuits are different only in terms of the frequency bandwidths of the variable and controlled oscillators.

The frequency bandwidths covered by the three signals are as follows, the figures being multiplied by three for the glide path.

(i)	Reflected signal	±90 Hz
(ii)	Re-radiated interference	±100 Hz (i.e. ±10 Hz on (i))
(iii)	Rogue interference	+300 Hz to -270 Hz

The variable reference oscillator is a voltage controlled oscillator the frequency of which can be varied locally by means of a potentiometer across a voltage supply. When switched to external the frequency can be programmed by means of an external variable voltage. The control laws for the three oscillators are shown in Figs.11 and 12.

A.5 <u>The glide path section (channels 1 and 2)</u>

The glide path channels are derived from the localiser drive circuits which, as have already been described, generate the required signals around the basic reference of 10 MHz.

The subsequent circuits which put the signals into the correct glide path channel are similar in design to the localiser section. The 10 MHz drive signals are each multiplied by three before being modulated with 90/150 Hz tones. The first local oscillator which determines the channel frequency is selected by a crystal in the frequency band 44.3 to 50 MHz whilst the second local oscillator operates on a frequency of 225 MHz to transfer the signals into the glide path band.

A.6 The marker section

A block diagram of the marker section of the simulator is shown in Fig.2.

It consists of a drive oscillator at 75 MHz feeding a modulator and thence through an amplifier and attentuator to the output.

There are three audio oscillators on the outer, middle and inner marker modulation frequencies of 400 Hz, 1300 Hz and 3000 Hz. The outputs from these oscillators are fed to linear gates where they are switched with square wave pulses obtained from logic circuits which provide the respective outer, middle and inner marker modulation codes. These outputs are then fed through three linear on/off gates before being connected to the modulator. Selection of either marker is obtained by operating the appropriate linear on/off gate with a -15 volt supply, zero volts being the off condition. When the simulator is switched to external the modulation tones can be obtained by applying zero volts and -15 volts to the appropriate control lines. The modulated RF can also be switched on and off either locally or externally the control in this case being a low impedance on the control line for the RF off condition and a high impedance for the on condition.

A.7 External input specification

A summary of the input requirements of the simulator when switched to external is given below:-

FACILITY		CONTROL
1 Localiser	Transmitter ident and timing	1 kHz, 4 kHz coded tones
2	Reflected signal RF on	Earthed line
3	Reflected signal frequency ±90 Hz	1 to 4.5 volts
4	Reflected signal amplitude 0 to -40 dB	0.8 to 1.5 volts
5	Reflected signal DDM guidance	90/150 Hz mixed tones
6	Re-radiated interference RF on	Earth line
7	Re-radiated interference frequency ±100 Hz	1 to 4.5 volts
8	Re-radiated interference amplitude 0 to -40 dB	0.8 to 1.5 volts
9	Rogue interference RF on	Earthed line
10	Rogue interference frequency +330 to -270 Hz	5.5 to 8.5 volts
11	Rogue interference amplitude 0 to -40 dB	0.8 to 1.5 volts
12 Glide Path	Reflected signal RF on	Earthed line
13	Reflected signal frequency ±270 Hz	
14	Reflected signal amplitude 0 to -40 dB	0.8 to 1.35 volts
15	Reflected signal DDM guidance	90/150 Hz mixed tones
16	Re-radiated interference RF on	Earthed line
17	Re-radiated interference frequency ±300 Hz	
18	Re-radiated interference amplitude 0 to -40 dB	0.8 to 1.35 volts
19	Rogue interference RF on	Earthed line
20	Rogue interference frequency +990 to -810 Hz	
21	Rogue interference amplitude 0 to -40 dB	0.8 to 1.35 volts
22 Marker	RF on	Open circuit line
23	Outer marker coded modulation on	-15 volts
24	Middle marker coded modulation on	-15 volts
25	Inner marker coded modulation on	-15 volts

Note: 13, 17 and 20 are controlled by inputs to 3, 7 and 10 respectively

Appendix B

PROGRAMME UNIT

The programme unit is composed of a number of self contained circuits each one being manufactured on a plug-in printed circuit board. These boards are mounted side by side across the unit behind a front panel which contains the necessary switches and lamps which operate the unit.

The individual circuit boards are described as follows reference being made to the overall block diagram Fig.13.

B.1 Speed/simulator interface Fig.14

The front panel mounted mean approach speed potentiometer is calibrated from 120 to 160 knots. The voltage drop across the potentiometer is arranged to be from -3 to -4 volts in order to drive the approach time ramp generator described later. The variable resistors for setting the speed calibration are mounted on the speed/simulator interface circuit board and are R1, R2-R3.

The radar Doppler shift in frequency of the reflected carrier received by the monitor is approximately 46 Hz to 61 Hz corresponding to approach speeds of 120 to 160 knots respectively. In order to provide the equivalent shift in frequency of the reflected carrier produced by the signal simulator, a voltage variation from 2.04 to 1.74 volts has to be supplied (Fig.11). This is carried out by the summing amplifier ML1 in the speed/simulator interface circuit.

The input, from the speed potentiometer slider, i.e. -3 to -4 volts, is fed into the non-inverting input of ML1 and the gain of the amplifier adjusted by means of R9 to be 0.3. The output will therefore vary from -0.9 to -1.2 volts. In order to arrive at the correct voltage required to operate the simulator, a negative input is applied to the inverting input of ML1 which is arranged to have unity gain. The output voltage is set by R5 to be 2.94 volts. This fixed voltage will sum with the output swing already produced, i.e. -0.9 to -1.2 volts, to give the required voltage swing at the output of 2.04 to 1.74 volts. This is then fed as a low impedance source to the aircraft reflected carrier drive oscillator control in the signal simulator.

B.2 Start time delay Fig.15

This circuit imposes a time delay between the operation of the START APPROACH switch and the beginning of the simulated approach. When the switch is

closed to earth the monostable ML1 operates for a period of time set by R2, the maximum being approximately 15 seconds. The positive leading edge of the pulse produced at the output of ML1 after the delay has operated is speeded up by ML2 and inverted before being fed into ML3. When ML3, a second monostable, is operated a negative pulse approximately 15 ms long is produced at pin 11 and is fed out to the SET line.

B.3 Approach time ramp generator Fig.16

This consists of a linear integrator followed by a voltage comparator. When an earth pulse is put on the reset line by the operation of the reset switch, ML3, a bistable, sets the condition such that output A is at zero and B is at a positive level. Transistor TR2 is cut off, relay AA/2 inoperative and therefore capacitors C1 and C2 are shorted out.

At the start of the approach, an earth pulse appears on the SET line which will switch ML3 to the opposite state. Transistor TR2 now conducts and the short circuit is removed from C1 and C2 allowing ML1 to integrate the negative input voltage across R3. This input voltage is derived from the speed potentiometer and for a speed setting of 160 knots R3 is adjusted such that ML1 will integrate to a maximum value over the required time period (Fig.4). The positive voltage ramp appearing at the output of ML1 is reduced in level by R10, R11 and fed to one of the inputs of the voltage comparator ML2. The other input is taken to the potentiometer R13 which is adjusted so that the positive voltage on the slider is just below the maximum level reached by the integrator. When these two voltages are equal the output of ML2 changes state from a positive logic level to zero, causing ML3 to switch to the reset condition. The output from ML1 falls to zero and the whole circuit remains in the reset condition until operated by the next SET pulse.

B.4 Range gate Fig.17

The range gates are used to select time periods along the voltage ramp produced by the approach time ramp generator. The ramp voltage is fed in on pin 28 and taken to the inverting input of ML2 and the non-inverting input of ML1 both of which are voltage comparators. The other two inputs of ML1 and ML2 are taken to potentiometers R1 and R3 across a 5 volt positive supply. When the ramp voltage is zero, the output of ML2 is zero and the output of ML1 positive. These two outputs are connected to two of the inputs of a twin 4 input NAND gate ML3 resulting in a positive output at pin 7 and an inversion through the second gate giving a zero output at pin 5.

As the ramp voltage rises positively a time will be reached when the input exceeds the level set by R3 at which point ML2 will change output state. The two inputs to the NAND gate will now be positive causing the outputs on pins 7 and 5 to reverse state.

The input ramp voltage continues to rise until it exceeds the level set by R1 when ML1 will change output state. The two inputs to the NAND gate are now at positive and zero levels again causing the outputs at pins 7 and 5 to revert back to positive and zero levels respectively.

Thus a pulse is produced which can be set over any time period of the simulated approach by means of R1 and R3. By putting an earth on pin 10, the gate ML3 is prevented from operating and the circuit can therefore be selected to operate on demand by means of a switch.

B.5 Marker/simulator interface Fig.18

Three range gates are used to produce pulses over the simulated approach corresponding to the time periods when an aircraft would be overflying the marker beacons. The marker/simulator interface circuit is used to convert the logic pulses produced by the range gates, into the -15 volt level required by the simulator linear gates and also to switch the 75 MHz marker RF.

The output of each range gate is fed to a corresponding emitter of an earthed base transistor the collector of which is connected to the signal simulator. The range gate output is normally positive causing the transistor to conduct and pull the collector down to earth. When the range gate operates, the output falls to zero, the transistor bottoms and the collector potential rises to -15 volts thus switching on the required modulation tone in the simulator.

Each of the three range gate outputs is also connected to the inputs of a NOR gate the output of which goes positive whenever any one of the range gates operate. This causes TR2 to conduct and relay MA/2 to operate removing the earth from the control line to the simulator and so switching on the marker RF for the duration of the range gate pulse.

B.6 Approach field strength curve generator Fig.19

This circuit board is designed to produce a field strength curve over the simulated approach path similar in shape to that obtained in practice. The linear ramp voltage obtained from the approach time ramp generator is fed into

a second integrator ML1. The shape of the output curve so produced is adjustable by variation of R3 and selection of C1 and C2. The integrator is allowed to integrate up to saturation level to produce a flat turn over to the curve. Just after saturation level has occured, transistor TR1 is switched into circuit. The base-emitter voltage is such that TR1 just starts to conduct causing C1 and C2 to discharge. As C1 and C2 discharge so TR1 conducts more heavily, the rate being controlled by adjustment of R10 to produce the shape required. The type of curve produced by this arrangement is illustrated in Fig.5.

The time along the simulated approach when TR1 conducts is controlled by R13 which sets the operating point of ML3. The voltage comparator ML3 is fed from the approach time ramp generator and uses identical circuitry to that described in B.3. The integrator start is controlled by relay contacts AA1 on the approach time ramp generator circuit board which are wired back across C1 and C2 on the approach field strength curve generator circuit board.

B.7 Localiser field strength/simulator interface Fig.20

This circuit board carries out the conversion of the voltage curve produced by the approach field strength curve generator into suitable levels for operating the voltage controlled attenuator in the signal simulator. It also switches ON the aircraft reflected carrier RF output from the signal simulator.

The approach field strength curve is a negative going voltage from zero and is fed across R1 and R2 the latter being adjusted to give a maximum swing into the summing amplifier ML1 from zero to -0.91 volts. In order to achieve a typical increase in reflected carrier level of 20 dB from the signal simulator, the voltage controlled attenuator requires a control variation from 1.3 to 1 volt positive Fig.8. The gains of both the non-inverting and inverting inputs of the summing amplifier are set at 0.33. The approach field strength curve voltage variation of 0 to -0.91 fed into the non-inverting input will therefore give an output of from 0 to -0.3 volts. When this input is at zero volts, the voltage fed to the simulator must be 1.3 volts. This is achieved by adjusting R3 for a voltage of -3.94 into the inverting input of the summing amplifier ML1 therefore producing 1.3 volts positive at the output. When the non-inverting input reaches -0.91 volts the output of -0.3 volts will sum with this fixed output of 1.3 volts giving the required 1 volt positive.

The second half of the circuit enables relay AC/2 to be operated ON when the approach is started and switched OFF at a point corresponding to the setting of R13 which together with ML2 and ML3 operate in a manner previously described.

The relay contacts are connected to the signal simulator circuits which make available the localiser and glide path reflected carrier RF. The glide path field strength interface operates in the same way and is described in B.11.

B.8 Sine waveform generator Fig.21

The sine waveform generator provides one of the two inputs required by the course line generator described in the next paragraph.

In the quiescent state a positive voltage obtained from R1 and R2 is applied through relay contacts AE/1 to the input of ML1 causing C1 to charge up giving a negative output across R7. ML2 and ML4 form a high speed switch. The negative level applied to the input of ML2 causes the output from ML4 to go negative and this in turn is fed via R14 to the input of ML2. The switching levels of ML4 are set by the biased diodes D6 and D7 such that the feedback voltage via R14 is below the maximum level to which C1 will integrate.

When the approach is started, relay AE/2 is operated, switching the input to ML1 from the fixed positive voltage to the negative voltage across R28. The capacitor C1 will now discharge in a linear manner to zero and then carry on charging positively. This positive output sums with the negative voltage fed back to the input of ML2 via R14. At the point where the positive output first exceeds the negative feedback voltage, the switch operates causing the input to the integrator to reverse. The circuit will carry on oscillating at a frequency determined by the setting of R28 until the relay contacts change over at the end of the approach.

The output across R7 is fed through a non-linear resistance R10, the current through which varies according to a square law. With an input of 10 volts applied to R10, the gain of ML3 is adjusted to unity by R19. The output e_o is therefore proportional to $-ke_i^2$ (Fig.22a) where e_i is the input voltage and $k = 0.1$.

If the triangular waveform input from R7 is adjusted to be ±5 volts, the output waveform from ML3 will be as shown by the solid line in Fig.22b. The output from ML3 is summed at the input to ML5 together with the driving

triangular waveform shown dotted in Fig.22b. The resultant output waveform from ML5, which closely approximates to a sinewave, is shown in Fig.22c.

Due to the initial charge of C1, the sinewave output will actually start from a peak value instead of zero, a condition which is required by the course line generator.

B.9 Course line generator Fig.23

The course line generator is designed to reproduce a dc course line voltage which varies around zero in a similar manner to an aircraft joining and approaching an ILS beam. The waveform is arrived at by multiplying the output from the sine waveform generator with a linear ramp function falling to zero over the approach the result being a damped sinewave output waveform.

The linear ramp function is obtained by summing in ML1, the approach time ramp generator output, which rises from zero to a maximum over the approach, with a negative potential obtained from R2. This potential is adjusted so that the output from ML1 reduces to zero at the end of the approach.

The ramp output from ML1 is fed via R8 to the X input of the multiplier ML2 and the sinewave via R9 to the Y input. By adjustment of R8 and R9 and the frequency of the sinewave, the shape of the resultant waveform at the output of the multiplier can be controlled.

Typical waveforms are shown in Fig.6. The output from the multiplier is connected across R12 so that the output swing can be set to a value convenient to the DDM generator.

B.10 Localiser DDM generator Fig.24

This circuit is designed to convert the dc course line produced by the course line generator into a differential variation of the 90 and 150 Hz audio signals for feeding to the localiser reflected carrier modulator in the signal simulator.

Two voltage controlled amplifiers ML3 and ML4 are used to perform this function, the phase locked 90 and 150 Hz input signals being obtained from the signal simulator. The gate voltage applied to each of these amplifiers is obtained from the amplifiers ML1 and ML2. In the absence of any signal at pin 30, i.e. zero DDM and the inverted input gain of ML1 and ML2 being unity, the output voltage levels can be set by means of R2. These levels, approximately 2.7 volts positive, will set the gain of the amplifiers ML3 and ML4 and also ensure that the gate levels are on the linear portion of the control curves.

The 90 and 150 Hz outputs from the amplifiers are summed at the input to the amplifier ML5, R22 being included to adjust the two tones for equality of level. The output of this amplifier is fed out, on pin 4 to the signal simulator the level being adjusted by the gain control R25 for 20% modulation of the localiser reflected carrier.

The dc course line variation around zero which is applied to pin 30 is fed to the non-inverting input of ML1 where it subtracts from the output level and summed at the inverting input of ML2 where it adds to the output level. Thus a differential variation in gate voltages is produced which can be equalised by means of R10.

The maximum amount of differential gain or DDM is controlled by R12 in the course line generator circuit and is readily adjusted in the reset condition when the course line dc off-set is at a maximum and steady.

B.11 Glide path reflected carrier and DDM/simulator interface Fig.25

This board consists of two separate circuits, a glide path reflected carrier level interface and a glide path DDM interface.

The glide path reflected carrier level circuit is formed by the amplifier ML2 which is fed at the non-inverting input by the output voltage from the approach field strength curve generator, the level being adjusted by R8. A variable negative voltage is fed into the inverting input and by suitable adjustment of both R8 and R9 the output level change can be made to simulate the change in received signal level at the monitor which occurs on the glide path frequency.

This output level is fed to the voltage controlled attenuator in the signal simulator.

The DDM interface is fed with the differential 90 and 150 Hz outputs produced by the localiser DDM generator. The two inputs are equalised under zero DDM conditions by R3 and summed at the inverting input of the amplifier ML1. The output of the amplifier is taken to the glide path reflected carrier modulator in the signal simulator, the level being set for 40% modulation by means of the amplifier gain control R6.

B.12 Overfly interference generator and simulator/interface Fig.26

The function of this circuit is to switch on the re-radiated interference RF in the signal simulator and starting with the oscillator frequency exactly

the same as the reflected carrier frequency, slowly diverge them as would be the case if the re-radiated interference was received in the landing aircraft via an aircraft taking off over the localiser transmitter.

The speed voltage, which controls the Doppler shift in frequency of the reflected carrier, is fed to the non-inverting input of the amplifier ML2. The output is fed to the signal simulator and the level is adjusted by means of R14 such that the frequency of the re-radiated interference oscillator is the same as the reflected carrier oscillator. Because C1 is shorted at this time the inverting input to the amplifier ML2 is zero.

The relay AD/2 and associated drive transistors TR1 and TR2 are fed from the output of a range gate of exactly the same design as described in B.4. This range gate can be pre-set to operate the relay during any period along the approach. When the relay operates, contacts 2 and 3 close to switch on the re-radiated interference carrier and contacts 22 and 21 open to allow C1 and the amplifier ML1 to integrate. The linear ramp voltage at the output of ML1 is fed to the inverting input of ML2 so that it subtracts from the output fed to the simulator and progressively changes the frequency of the oscillator. The rate of change of frequency is controlled by the setting of R5.

A positive voltage adjustable by means of R2 is fed out to the voltage controlled attenuators in the simulator to set the RF level of the re-radiated interference.

The interference is selected by a front panel mounted indicator switch the upper half of which marked OVERFLY INT lights up when selected. This removes the inhibit from the range gate allowing it to operate over the pre-selected period. To indicate this period the lower half of the indicator marked AIRCRAFT OVERFLYING lights up.

B.13 G/P - loc rogue interference generator and simulator interface Fig.27

This interference generator is designed to produce a fixed, or sweep frequency interference in either the glide path or localiser spectrum. The fixed interference can be adjusted both in frequency and amplitude by means of front panel mounted controls. The sweep interference moves in frequency right through the spectrum being monitored at a pre-set rate, the amplitude being adjustable by means of a front panel mounted control.

The rogue frequency oscillator in the signal simulator which is controlled by this circuit is common to both the localiser and glide path drive sections. Selection of the appropriate channel on which the interference is required is therefore carried out by routing the RF ON/OFF relay connection from pin 19 through to the simulator localiser and glide path relays via a selector switch mounted on the front panel and marked LOCALISER - GLIDE PATH.

The relay RA/2 is driven from a lamp driver circuit which in turn is fed from a range gate. The relay can therefore be switched ON over any period of the approach by adjustment of the range gate. When the relay operates contacts RA/1 remove the short circuit from the integrating capacitor C1 and contacts RA/2 put an earth on the line which switches on the rogue interference RF in the selected channel. The capacitor C1 integrates at a rate determined by the setting of R7. The negative voltage ramp which appears at the output of ML1 is summed at the inverting input of ML2 with a negative voltage which can be varied by means of R14. The output of ML2 consists therefore of a positive ramp starting from a fixed positive voltage, the levels being adjustable to give the required frequency coverage from the simulator.

When relay RB/2 is not operated the ramp voltage will be fed to the simulator via contacts RB/2 and pin 15. At the same time, a positive voltage is fed to the RF voltage controlled attenuators via contacts RB/1 and pin 13. This voltage and consequently the RF level can be adjusted by the front panel mounted potentiometer wired across pins 30 and 4.

When relay RB/2 is operated, i.e. in the fixed frequency mode, the oscillator voltage control is disconnected from the ramp source by contacts RB/2 and connected to the front panel mounted potentiometer wired across pins 29 and 3. The oscillator frequency can thus be pre-set anywhere in the monitor spectrum. Relay contacts RB/1 also change over and select the output from the front panel mounted potentiometer connected across pins 31 and 6 so that the RF level of the fixed frequency interference can be adjusted independently.

The two indicator switches mounted on the front panel which select either the fixed or sweep interference are cross wired so that they cannot be operated together. The upper halves of the indicators are marked FIXED FREQ. INT and SWEEP FREQ. INT and these light up when the appropriate switch is operated and removes the inhibit from the range gate. When the range gate operates, the lower half of the indicator marked ON lights up during the pre-set period.

B.14 Ident. pulse generator Fig.28

The uni-junction TR1 and the associated components form a pulse generator which produces a pulse every 120 ms. This pulse train is fed to the NAND gate ML1(a) which acts as the necessary interface to drive the appropriate micro-logic elements. The output of ML1(a) is used to drive two decade counters ML3 and ML4, connected in cascade to form a divide by 100 counter. The output is also taken off the circuit board via pin 2 in order to drive the timing pulse generator described later.

The BCD outputs from the counters are cross connected to two BCD-Decimal converters ML5 and ML6. Only the necessary decimal output pulses required by the ident. code generator circuit are taken out from the BCD-Decimal converters.

This circuit board also contains the elements ML1 and ML2 which provide the setting and re-setting levels for most of the logic circuits. ML1(b) consists of two NAND gates cross connected to form a dc coupled flip-flop. When the RESET switch is operated, an earth pulse appears on the reset 1 line at pin 11. This causes the output at pin 6 (reset 2) to go positive and the output at pin 10 (reset 3) to go negative, the condition being held after the reset 1 pulse has disappeared. When the start approach switch is operated, an earth pulse appears on the start line at pin 3. This causes the flip-flop to change state putting a negative level on the reset 2 line and a positive level on the reset 3 line. When the reset 2 line changes state from positive to negative, the monostable ML2 operates and produces a positive pulse approximately 5 ms long on the pre-set line at pin 9.

B.15 Ident. code generator Fig.29

The ident. code generator is designed to reproduce the runway identification codes ILL or IRR corresponding to runways 28 left and 28 right at London Airport, Heathrow.

The decimal output pulses from the ident. pulse generator are fed into two hex.inverters ML1 and ML2. The positive pulses so obtained are then fed into the NAND gates formed by ML3, ML4, ML5 and ML6 which select by means of a wired OR function the pulses to form the code characters.

The selection of the particular code required is performed by the first two gates of ML7 acting as NOR gates. The common pulses of each code are fed to both NOR gates, the remaining pulses being fed to the other input of the

corresponding gate. The output of each gate in the form of positive pulses is selected by the front panel mounted switch marked 28L, 28R which connects via a lamp driver circuit to the upper indicator on the same switch marked IDENT ON causing it to flash the code selected.

The time interval between codes is approximately 7.68 seconds corresponding to 64 pulses. The decimal outputs 4 and 60 are therefore fed into the third gate of ML7, used as a NAND gate, which produces a negative output pulse after 63 driving pulses to the counter. This output pulse is inverted in the fourth gate of ML7 to provide a positive pulse on the set zero line which is fed back to the counters in the ident. pulse generator circuit to reset them to zero. The second input to this gate is connected to the reset 3 line which, as has previously been described, is held negative until the start approach switch is operated. This has the effect of holding the set zero line positive and inhibiting the counters.

The two pulse codes produced are shown in Fig.30.

B.16 <u>Timing pulse generator Fig.31</u>

The timing pulse generator consists of two decade counters ML1, ML2 and a divide by five counter ML3 connected in cascade to form a divide by 500 counter. This counter is driven by the 120 ms pulse rate from the ident. pulse generator circuit to give a clock pulse output at pin 7 every minute. The outputs from the two decade counters are cross connected to two BCD-Decimal converters ML4 and ML5. The decimal outputs required for the timing code generation are inverted through ML6 and ML7. Three of the inverters in ML7 are used as a NAND gate and are connected direct to the outputs of the divide by five counter ML3 in such a way as to provide a positive pulse at pin 5 the length of which corresponds to the pulse count from 1 to 100. The set zero inputs to the counters are connected together and are fed from the reset 2 line which changes from a positive to a negative state when the start approach switch is operated thus removing the inhibit from the counters.

B.17 <u>Timing code generator Fig.32</u>

The timing code generator is designed to produce a three letter morse code sequence which is transmitted once every minute, the last letter in the sequence changing to indicate the time change of one minute. The code is used at London Airport on runway 28L the first letter indicating hours, the second, tens of minutes and the third, minutes, the characters used being Z for O, A for 1, B for 2, etc.

The required decimal outputs from the timing pulse generator are fed into the NAND gates ML1, ML2, ML3 and the first two gates of ML4 to form the pulse lengths required for the timing characters. The outputs from the NAND gates are fed into the NOR gates ML5(a), ML7 (two gates) and ML5(b) to form the morse code characters TEE, TEF, TEG, TEH, TE1 corresponding to times of 2055, 2056, 2057, 2058 and 2059 hours. The five outputs from these gates are fed into five NAND gates ML5(c) and ML8 the outputs from which are joined and fed to the input of the fourth gate in ML8 to give an inversion. The final output at pin 22 is therefore in the form of a train of positive pulses Fig.30.

The sequencing of the five sets of timing characters is carried out by the 5 bit shift register ML9. The 5 outputs from the shift register are connected to the second inputs of the NAND gates ML5(c) and ML8. In the reset condition, the reset 3 line connected to the shift register is held negative thus clearing and inhibiting the register. All five outputs from the register are negative in this condition thus preventing any of the NAND gates from giving an output. When the start approach switch is operated the reset 3 line changes to a positive level allowing the shift register to operate. At the same time the positive pulse generated in the ident. pulse generator circuit is applied to the input of the first flip-flop in the register via the pre-set line, the delayed negative edge changing the first output from the register to a positive state. This allows the first NAND gate in ML5(c) to operate and produce the first code letters TEE. When the counter in the timing pulse generator circuit has counted up to one minute, a clock pulse is generated which is inverted to the correct polarity in ML4 and applied to the shift register. The effect of this is to cause the second flip-flop in the register to change state so putting a positive level on the second NAND gate in ML5(c). As the output of the last stage of the register is connected back to the input, the first flip-flop will also change state and now inhibits the first NAND gate in ML5(c). Thus only the second code TEF is generated in the output.

The sequence is carried on, the code changing every minute until the shift register is finally cleared by the reset 3 line after a landing has been run through.

The timing code is selected by a front panel mounted switch marked TIMING ON which removes an earth across the output at pin 22. The code is also connected via a lamp driver to the lower half of the switch indicator marked CODE causing it to flash the timing code.

B.18 1020/4000 Hz gated oscillator Fig.33

The identification and timing signals appear on the ILS localiser transmitter as low level modulation frequencies of 1020 Hz and 4000 Hz respectively.

The 1020/4000 Hz gated oscillator circuit is designed to generate these two frequencies the outputs being gated by the ident code and timing code generators before being fed to the signal simulator as a modulation on the transmitter reference and reflected carrier RF signals. The component values for the two circuits, with the exception of the frequency determining capacitors C1, C2 and C3 in the oscillator sections, are identical.

The transistor TR1 is connected as a phase shift oscillator, final adjustment of the frequency being obtained by R3. The feedback is adjustable by means of R8 to the point of minimum distortion consistent with maximum output. The oscillator is followed by an emitter follower TR2 the output from which can be controlled by means of R11. This potentiometer serves as a depth of modulation control of the carrier generated by the signal simulator. This output is fed to a gated amplifier ML1 which has a gain of some 20 dB when the gate input is at a positive logic level and -70 dB when it is at zero.

The positive pulse trains from the ident. code and timing code generators are connected to the gate inputs of the 1020 Hz and 4000 Hz amplifiers respectively. The input to the signal simulator therefore consists of coded bursts of 1020 Hz and 4000 Hz in accordance with the code selected.

B.19 Aircraft landed logic Fig.34

This circuit is designed to flash the aircraft landed indicator at the end of an approach.

It consists of a uni-junction TR1 producing pulses every 330 ms which after inversion through ML1(a) are applied to the input of the flip-flop ML3. The square wave output obtained from ML3 is fed into the first NAND gate of ML1(b). The second input to this NAND gate is fed from the monostable ML2 the output from which is normally negative until it is operated.

A level change from negative to positive is produced at the output of ML2 in the approach time ramp generator at the end of the approach when the circuit resets to zero. This level change is fed into the aircraft landed logic circuit at pin 14 where it is inverted by ML1(c) and used to trigger

the monostable ML2. When the monostable operates, the output polarity changes for approximately 5 seconds allowing the first NAND gate in ML1(b) to operate and produce negative pulses during this period. These pulses are inverted by the second gate in ML1(b) before being fed out via a lamp driver circuit to the lamps in the indicator marked AIRCRAFT LANDED.

B.20 Lamp drivers Fig.35

The lamp driver circuit board contains fourteen transistor drive circuits which are used throughout the programme unit to drive the lamps contained in the indicator switch units.

B.21 Internal switches Figs.13 and 36

These are four toggle switches mounted on the top of the side members which carry the printed circuit boards.

The first two switches marked 1 kHz and 4 kHz are used to switch the gate inputs to the 1020/4000 Hz gated oscillator circuit board from the coded input to the +5 volt line. When the switch is operated, the indicator on the appropriate switch will be continuously lit and a steady tone applied to the signal simulator for setting up the depth of modulation.

The third switch marked DDM, disconnects the course line dc and earths the input to the localiser DDM generator so that both the zero DDM and depth of modulation can be set up using the signal simulator.

The fourth switch marked BT, removes the earths on the control lines to the simulator thus breaking the relays which normally feed the breakthrough signal from the reference across to the reflected signal channel on both localiser and glide path outputs. This is included to allow the individual reflected signal levels to be set up and measured at the simulator.

B.22 Power supplies Figs.13 and 36

Two commercial twin output power units are used in the programme unit mounted on their side at the rear. They are mains input fused with a 2 amp fuse on the front panel and switched by means of a push ON/push OFF switch and indicator marked MAINS ON. The output voltages are +28 volts, +20 volts, +5 volts and -20 volts relative to earth and are all short circuit protected, the maximum current capability on each output being 1 amp.

REFERENCE

No.	Author	Title, etc.
1	T.R.G. Lampard	Radio environment monitoring for the category III instrument landing system. RAE Technical Report 70076 (1970)

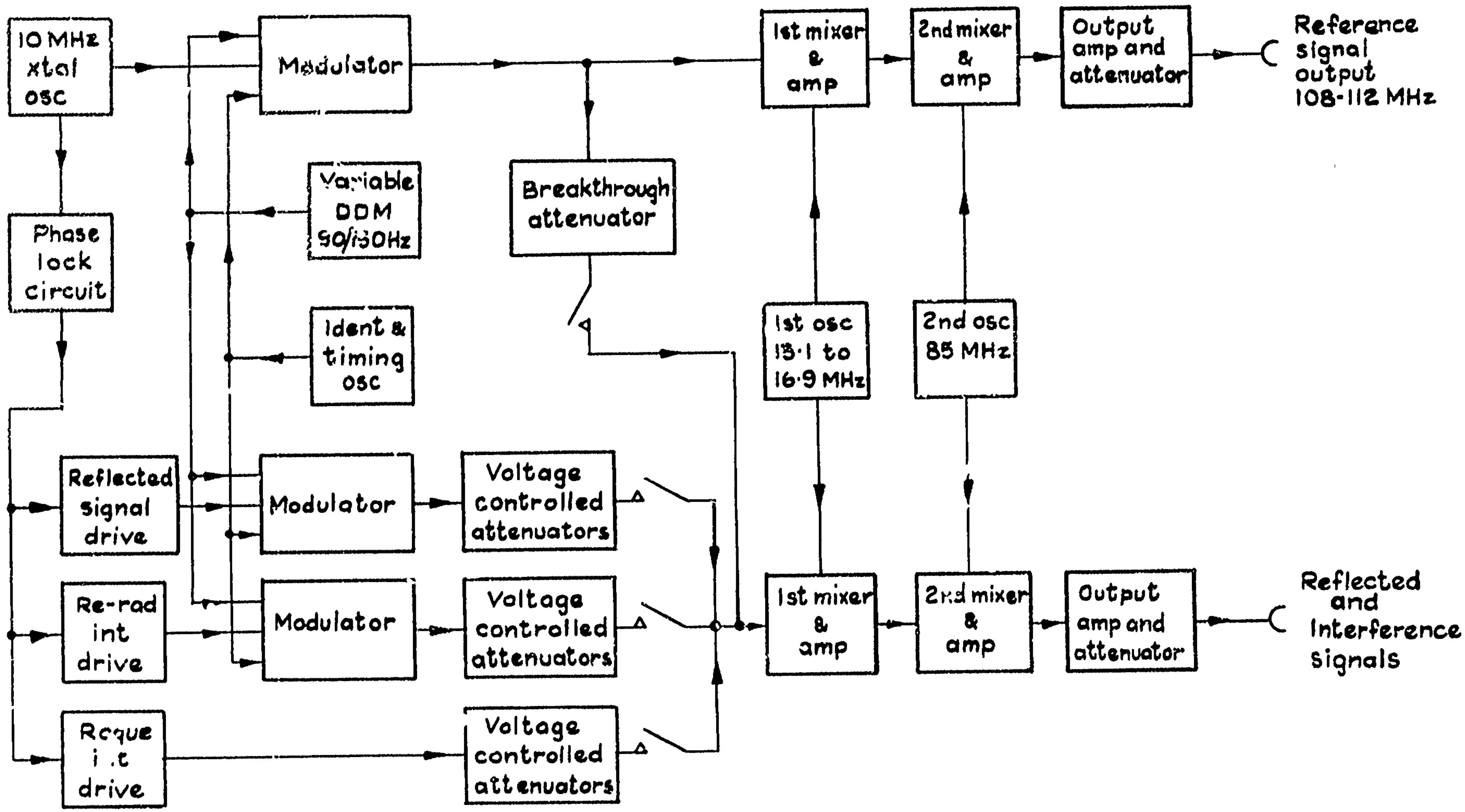

Fig.1 Signal simulator-localiser section

Fig. 1

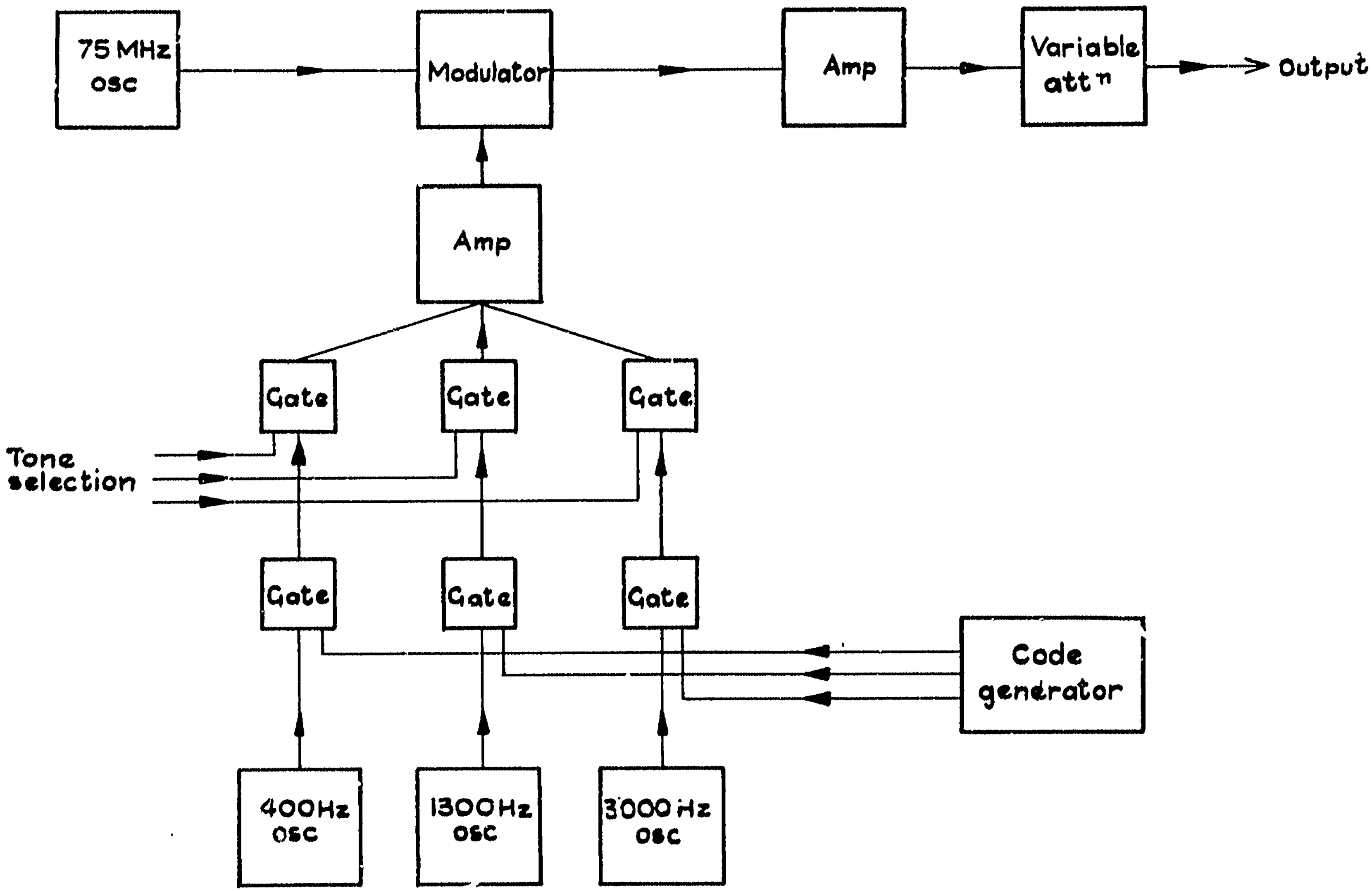

Fig. 2 Signal simulator marker section

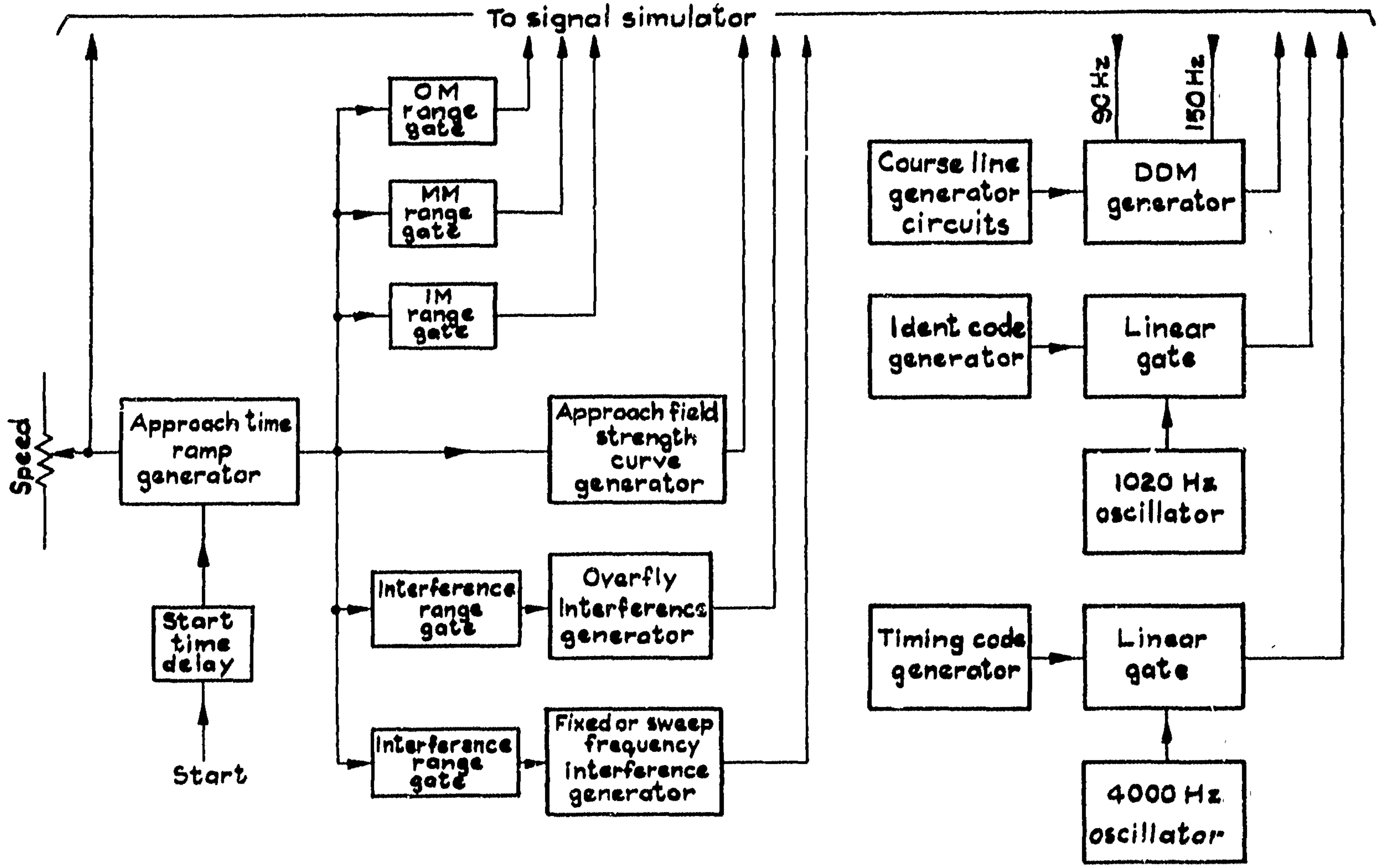

Fig. 3 Simplified block diagram of programme unit

Fig. 3

Fig.4

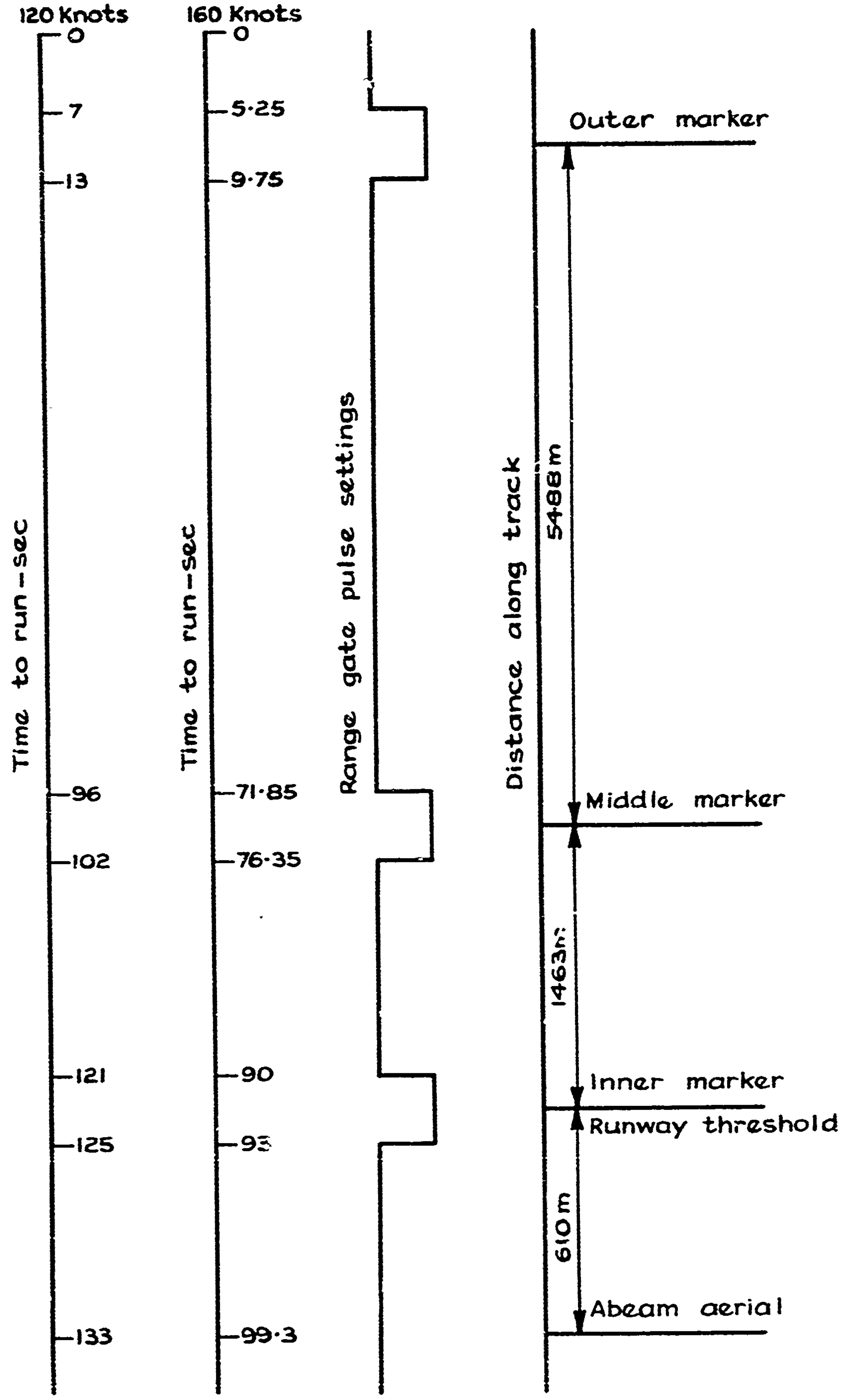

Fig.4 Time and distance chart runway 28 L

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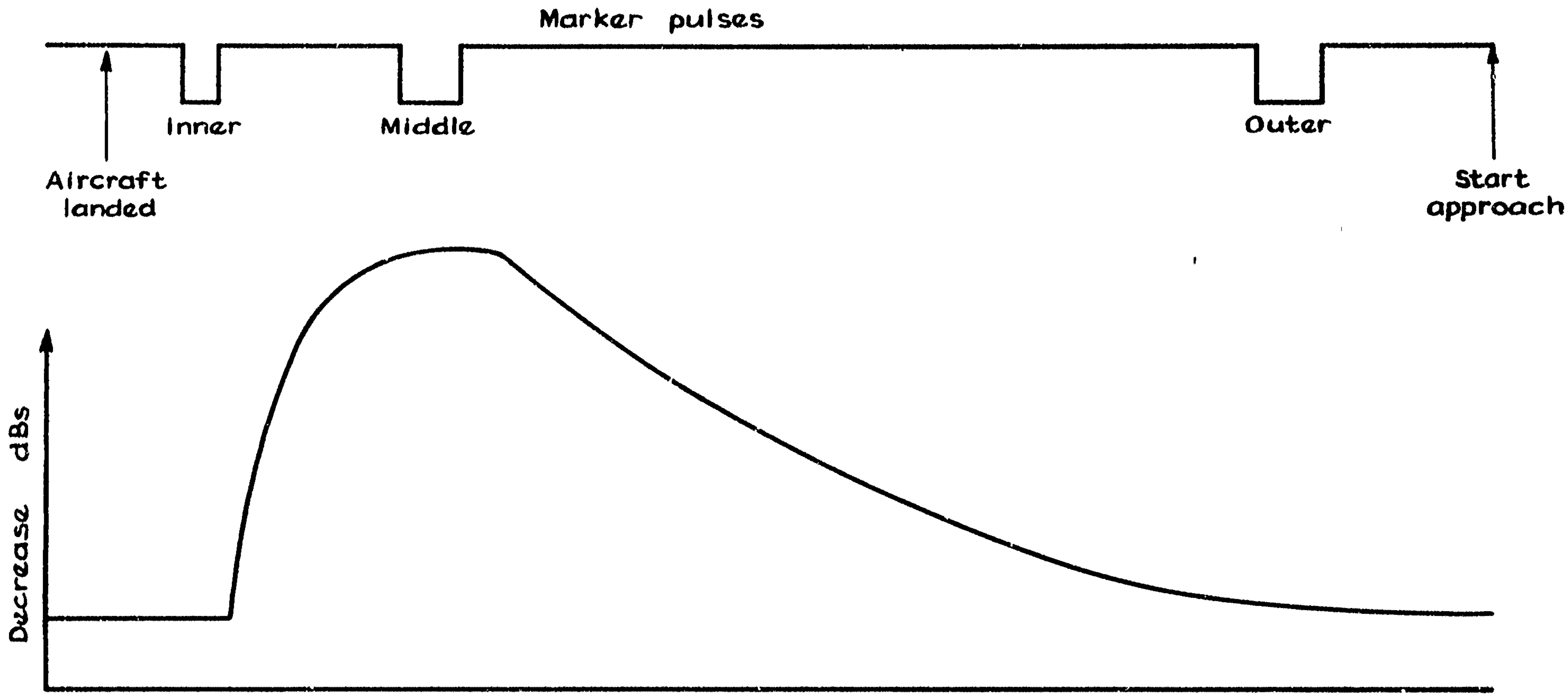

Fig. 5 Approach field strength curve generator output waveform

Fig. 5

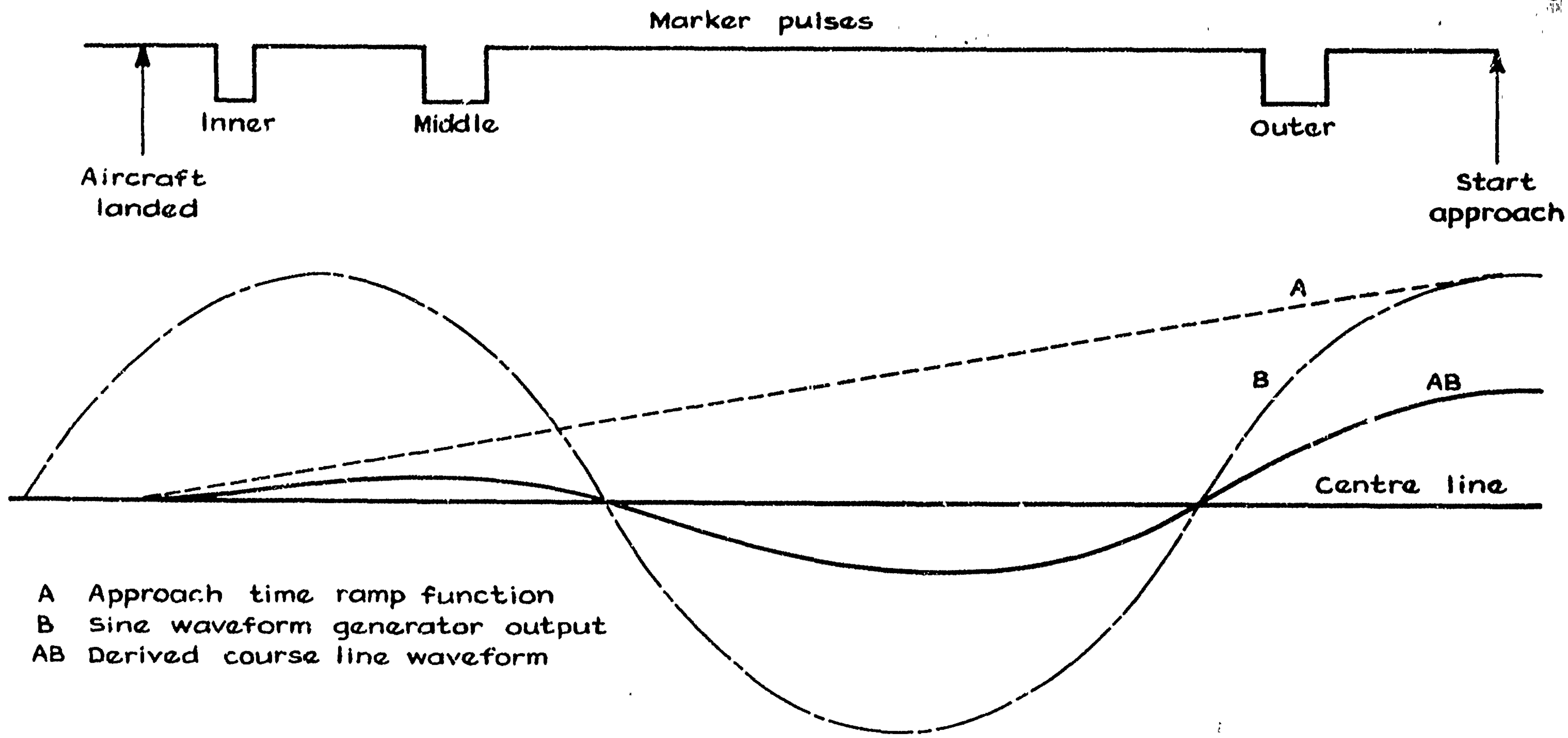

Fig.6 Course line generator output waveform

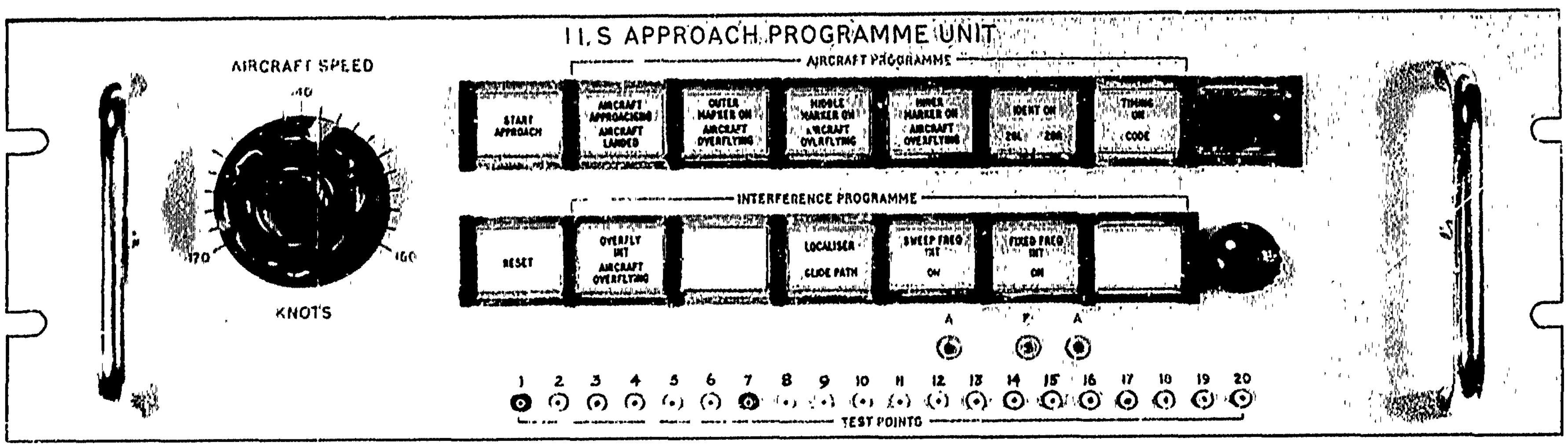

Fig.7. I.L.S. approach programme unit, front view

Fig. 8

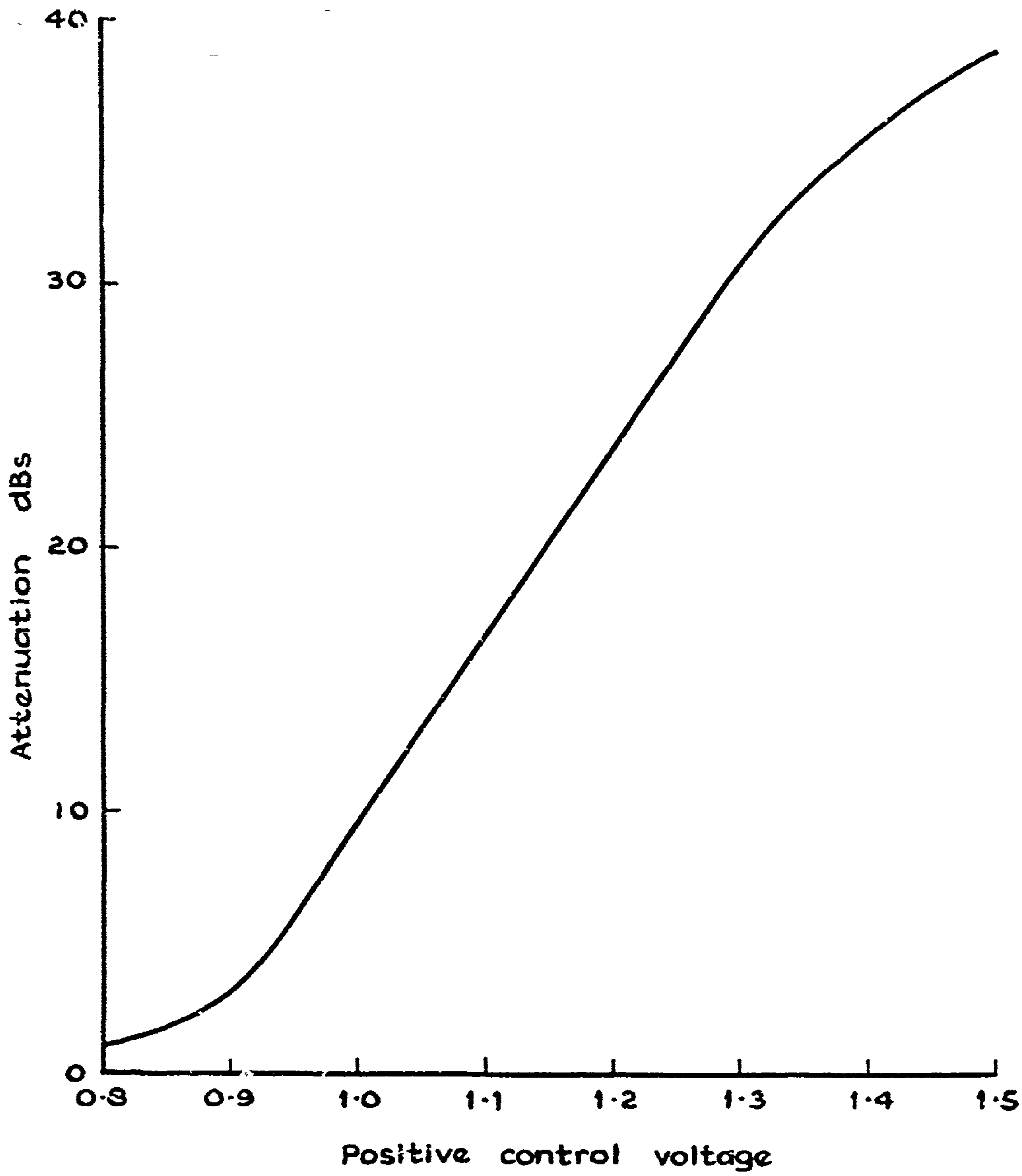

Fig. 8 Calibration of localiser attenuaters

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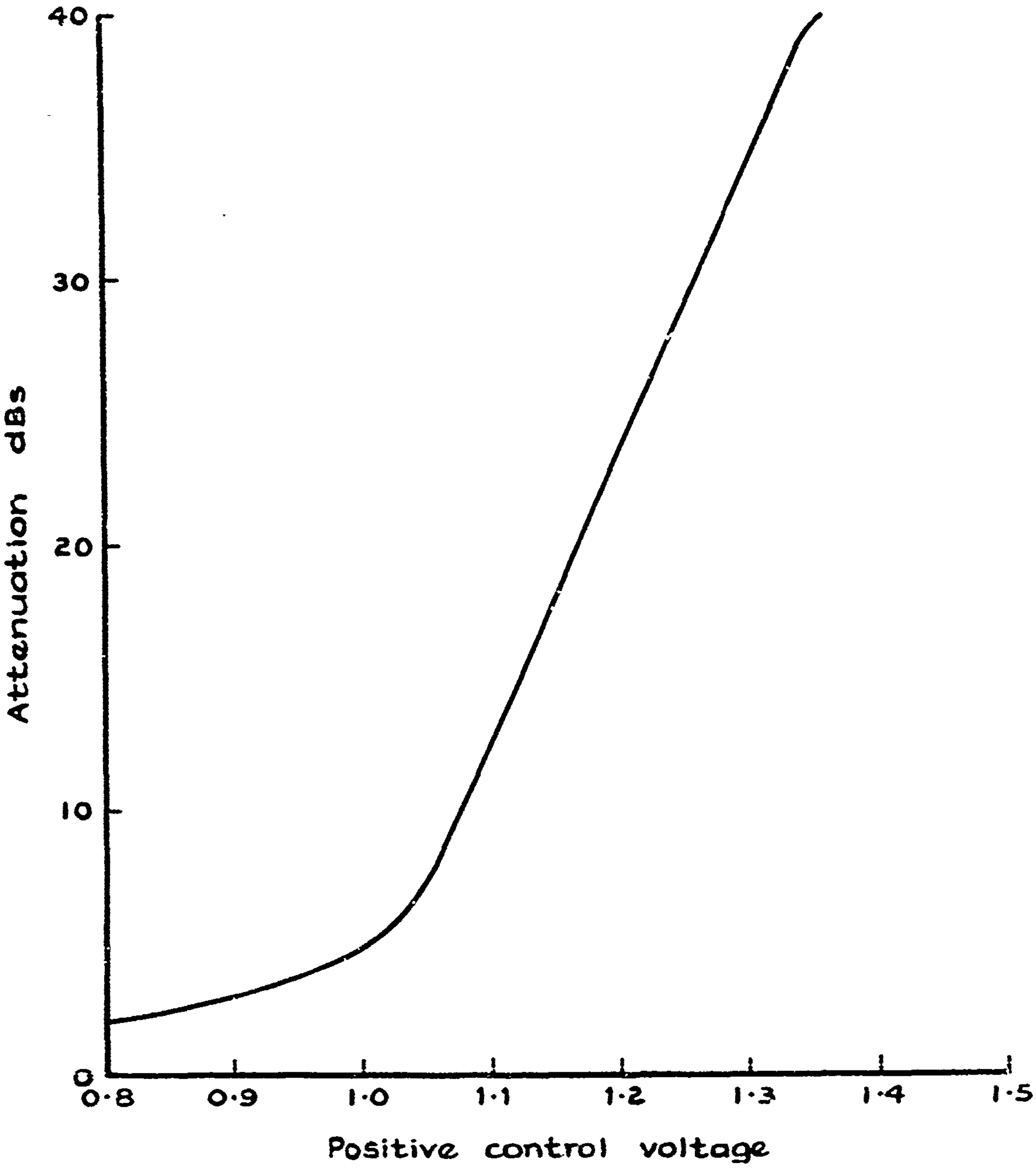

Fig.9 Calibration of glide path attenuators

Fig. 10

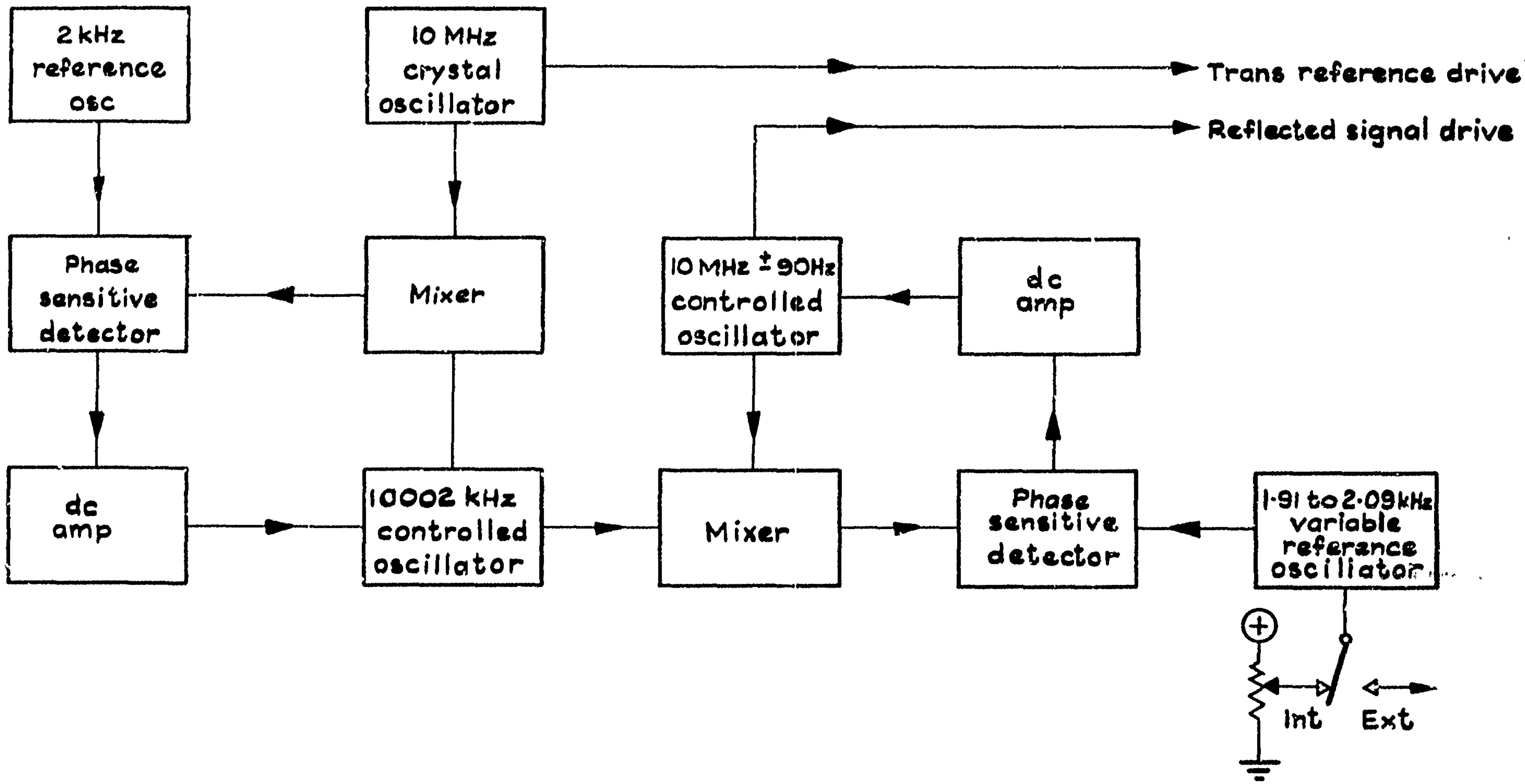

Fig. 10 Drive circuit reflected signal

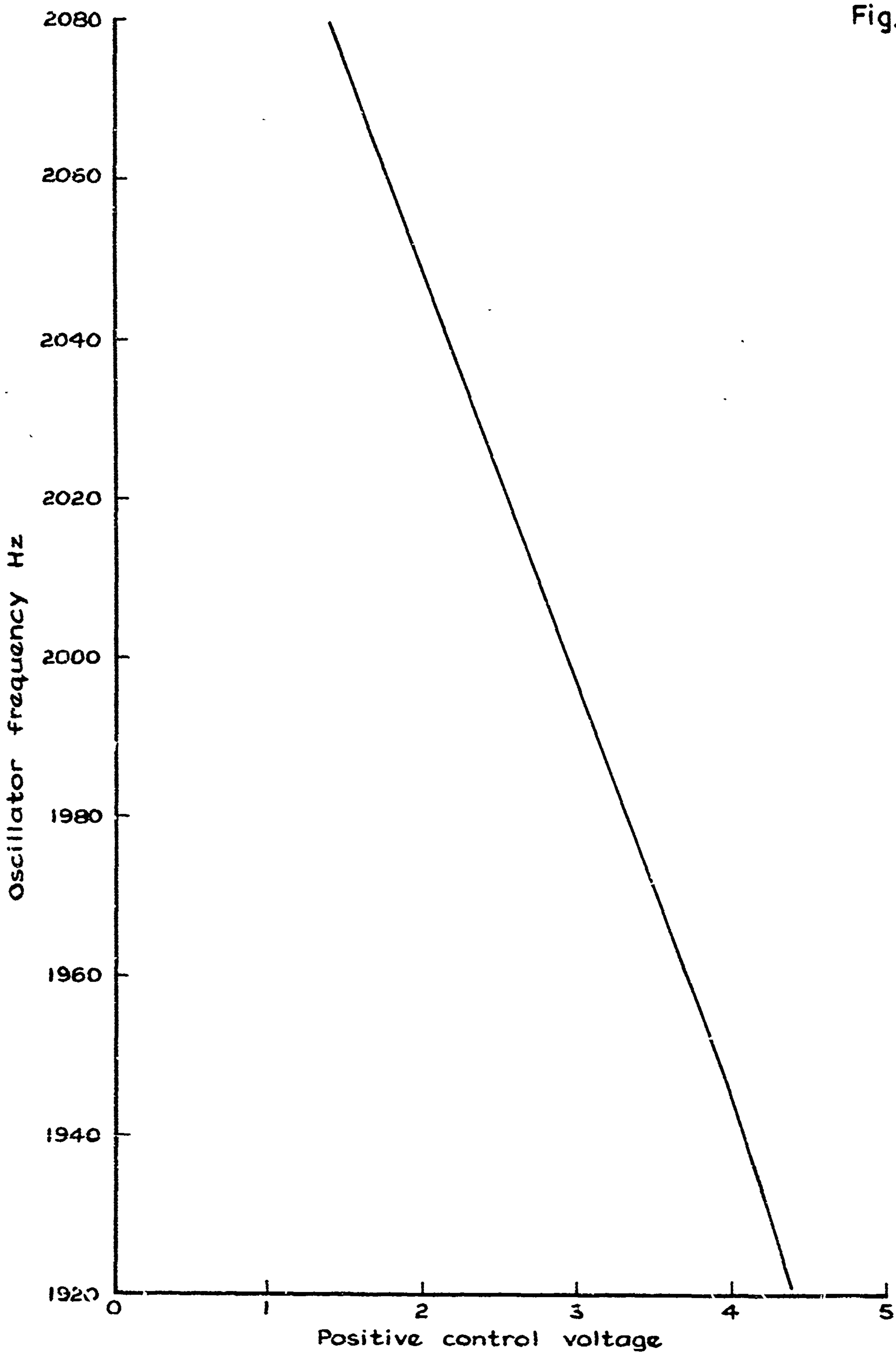

Fig.11 Calibration of reflected signal and re-radiated interference oscillators

Fig.12

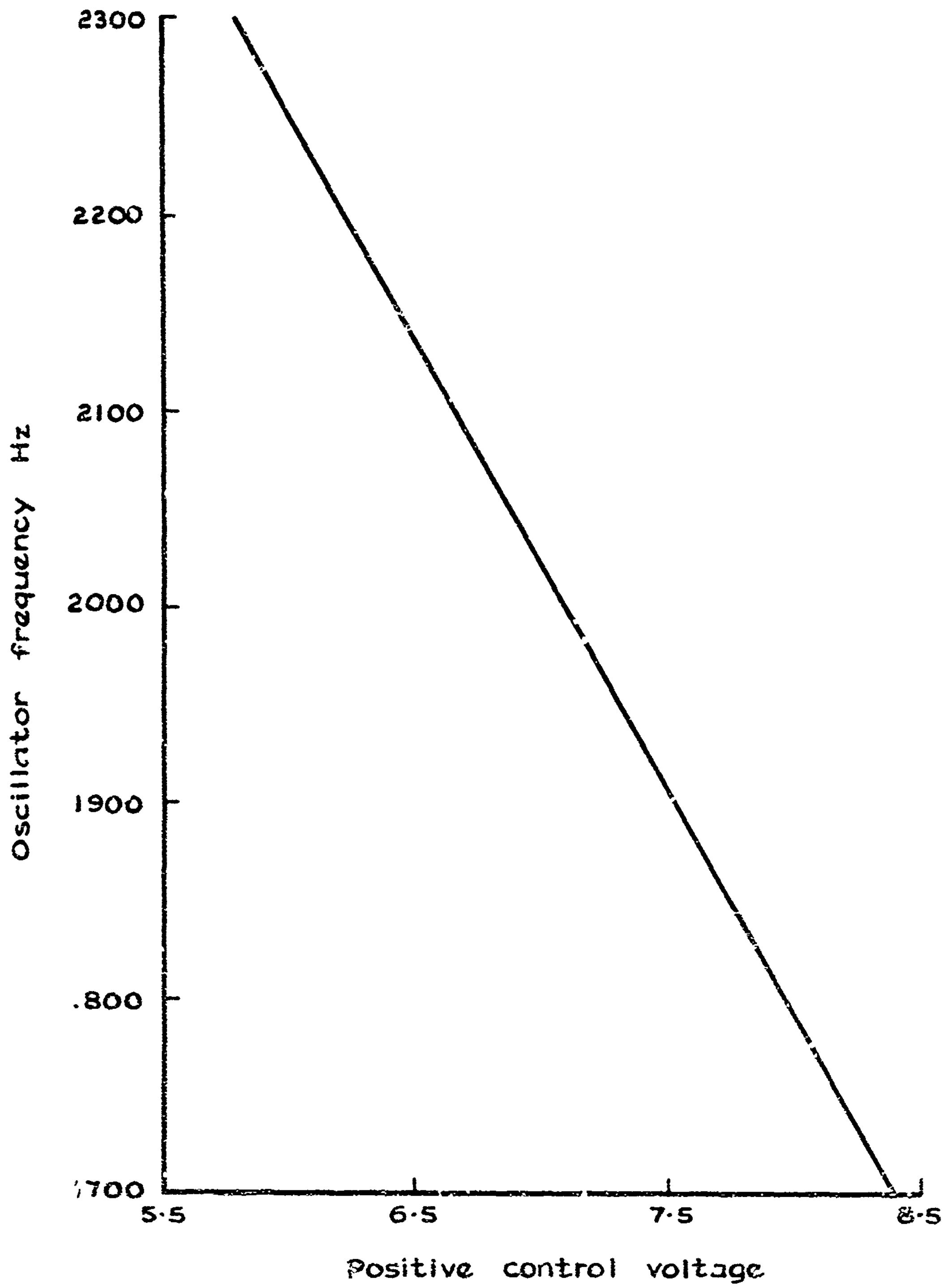

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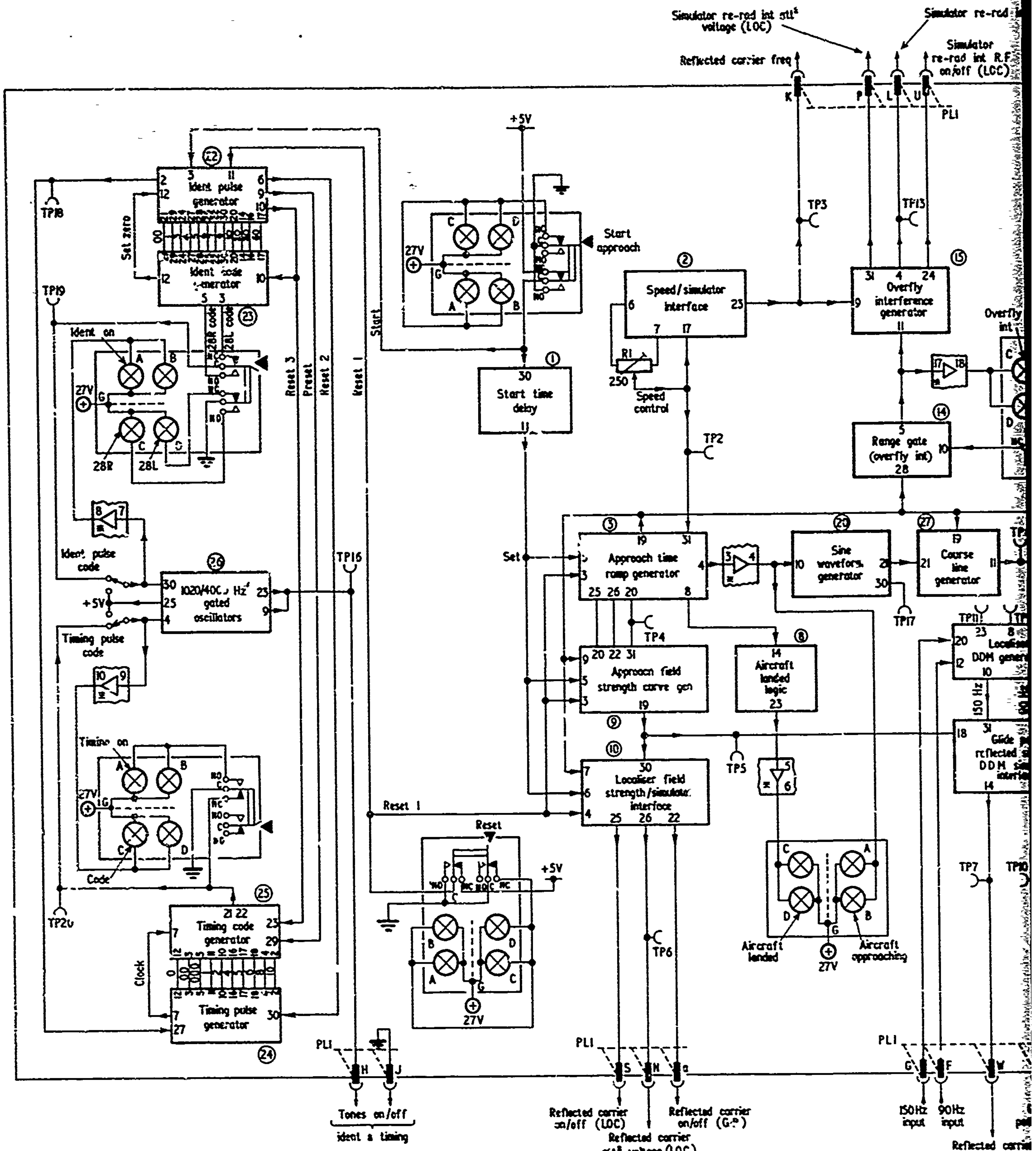
Fig.12 Calibration of rogue interference frequency oscillator

A



T.R. 71145

⌗ Board No 19

⑥ Board designation

Nos 11 21 & 28 spare boards

Fig.13 ILS approach programme

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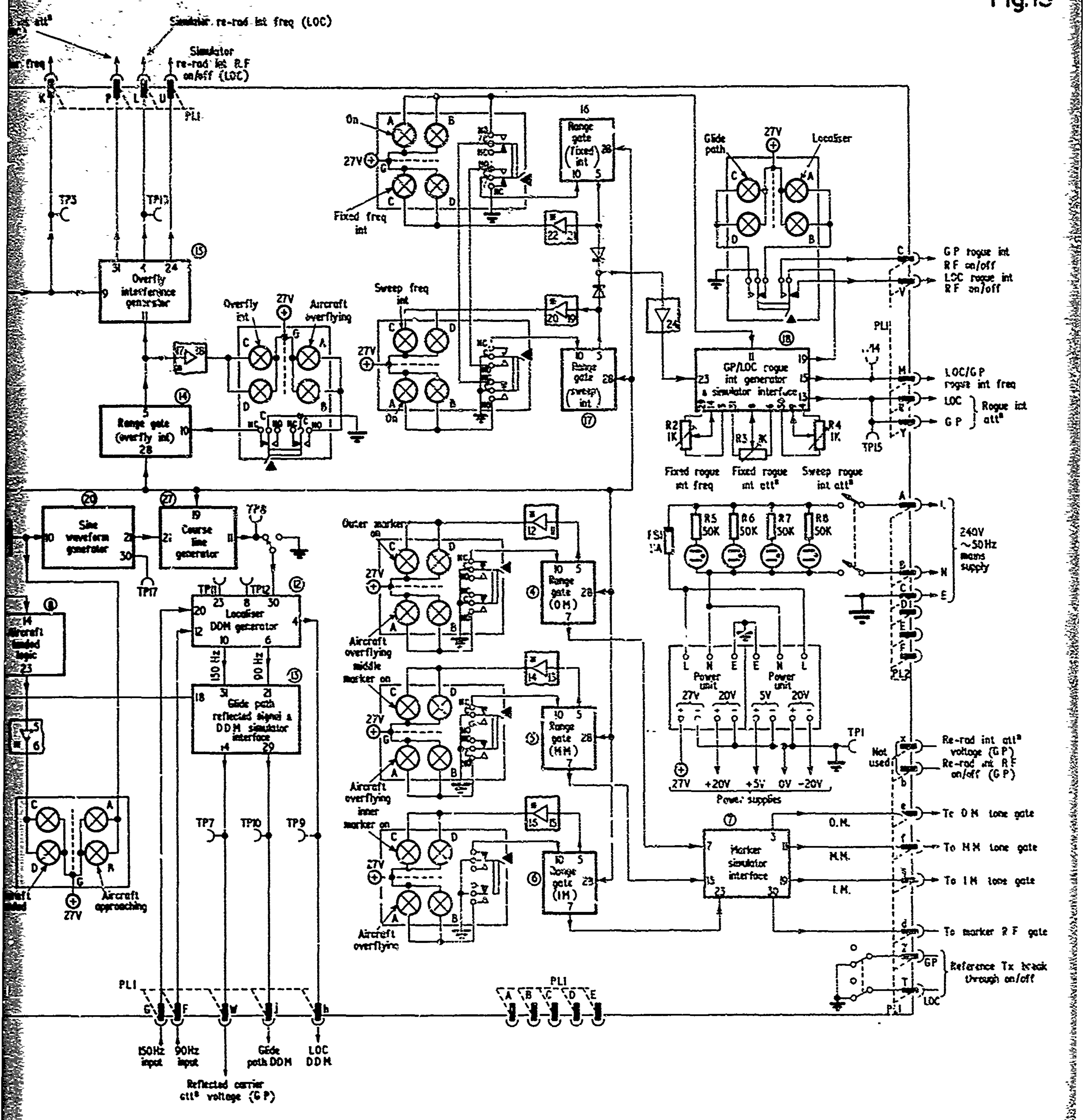
B

Fig. 13



approach programme unit - block diagram

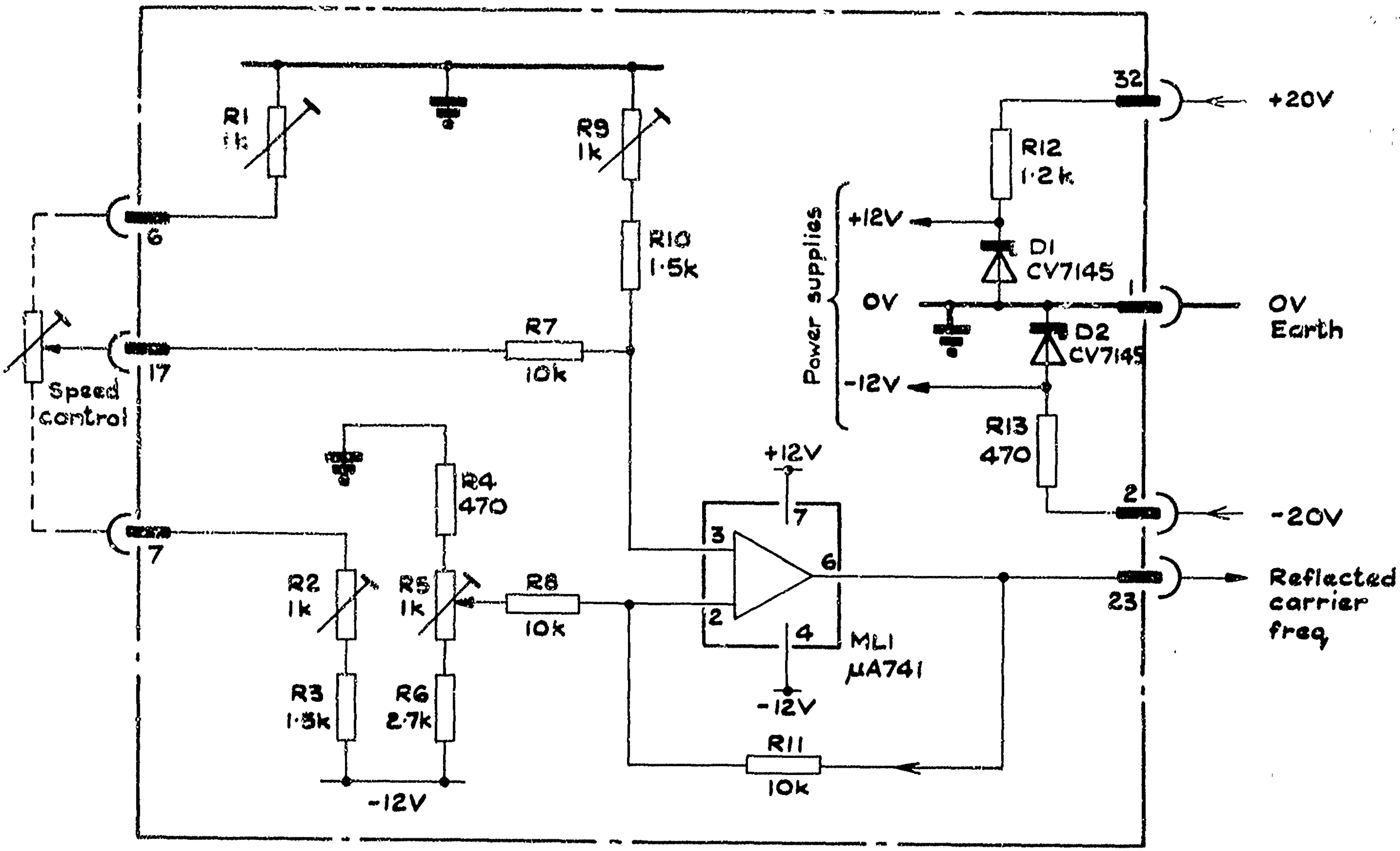


Fig. 14 Speed/simulator interface-circuit diagram

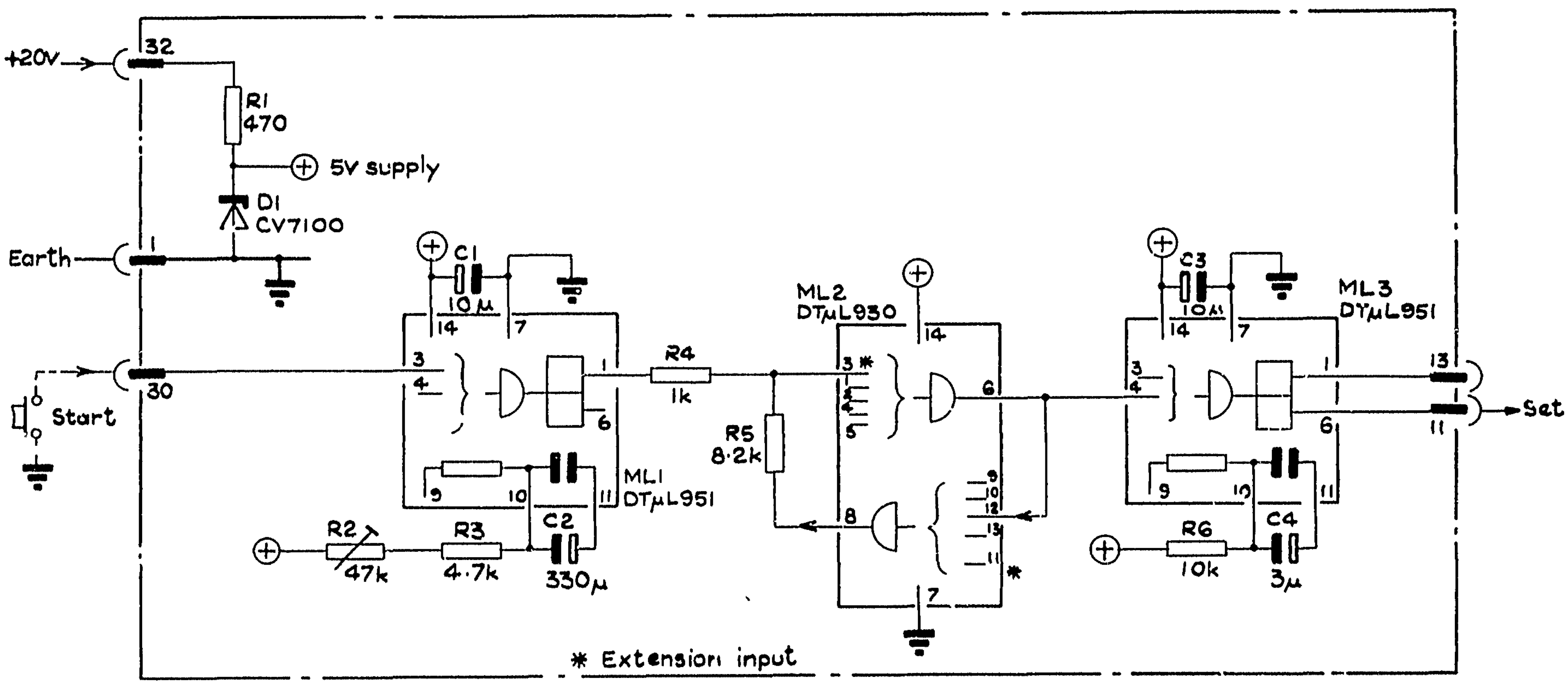


Fig. 15 Start time delay-logic diagram

Fig. 16

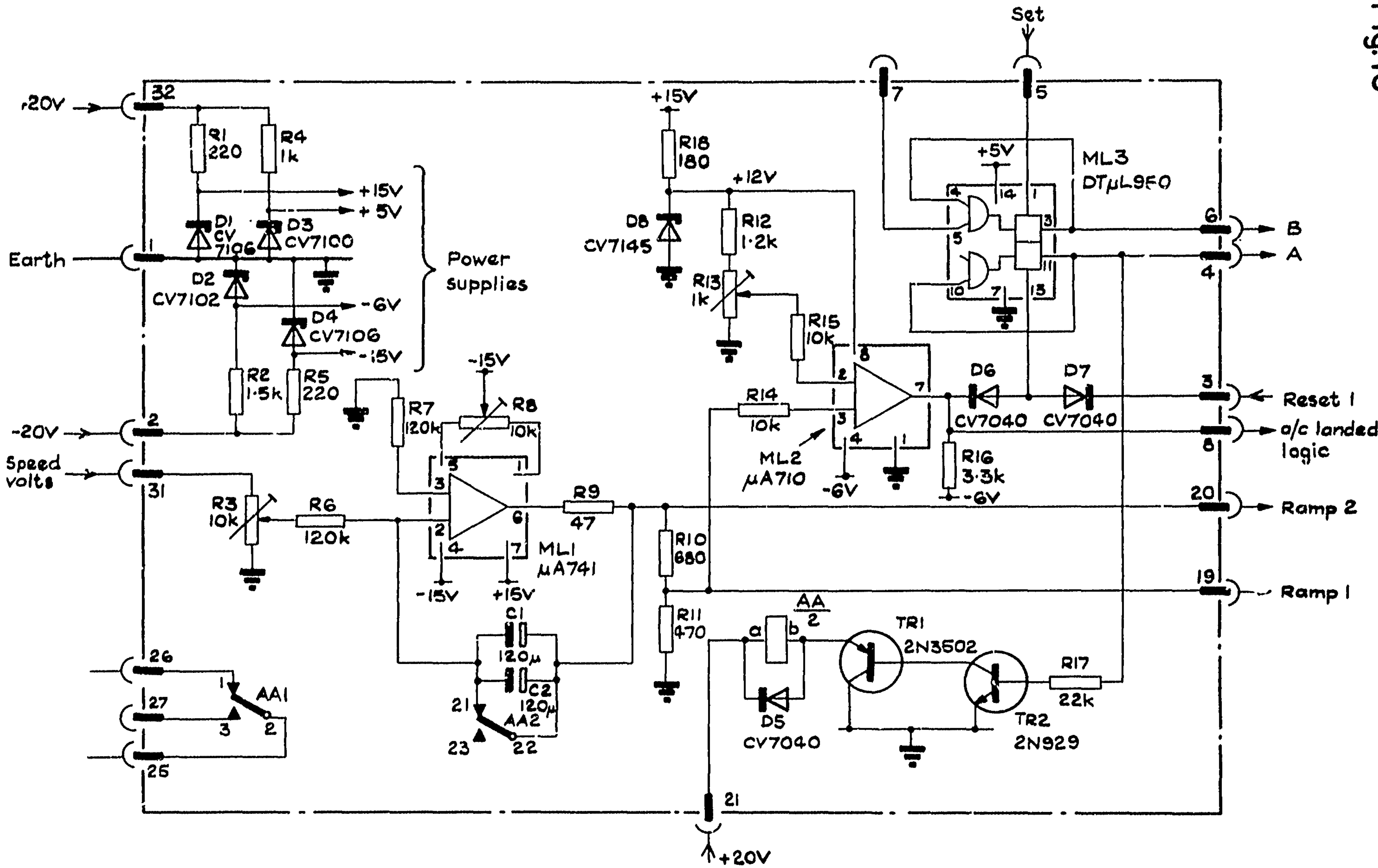


Fig. 16 Approach time ramp generator-circuit diagram

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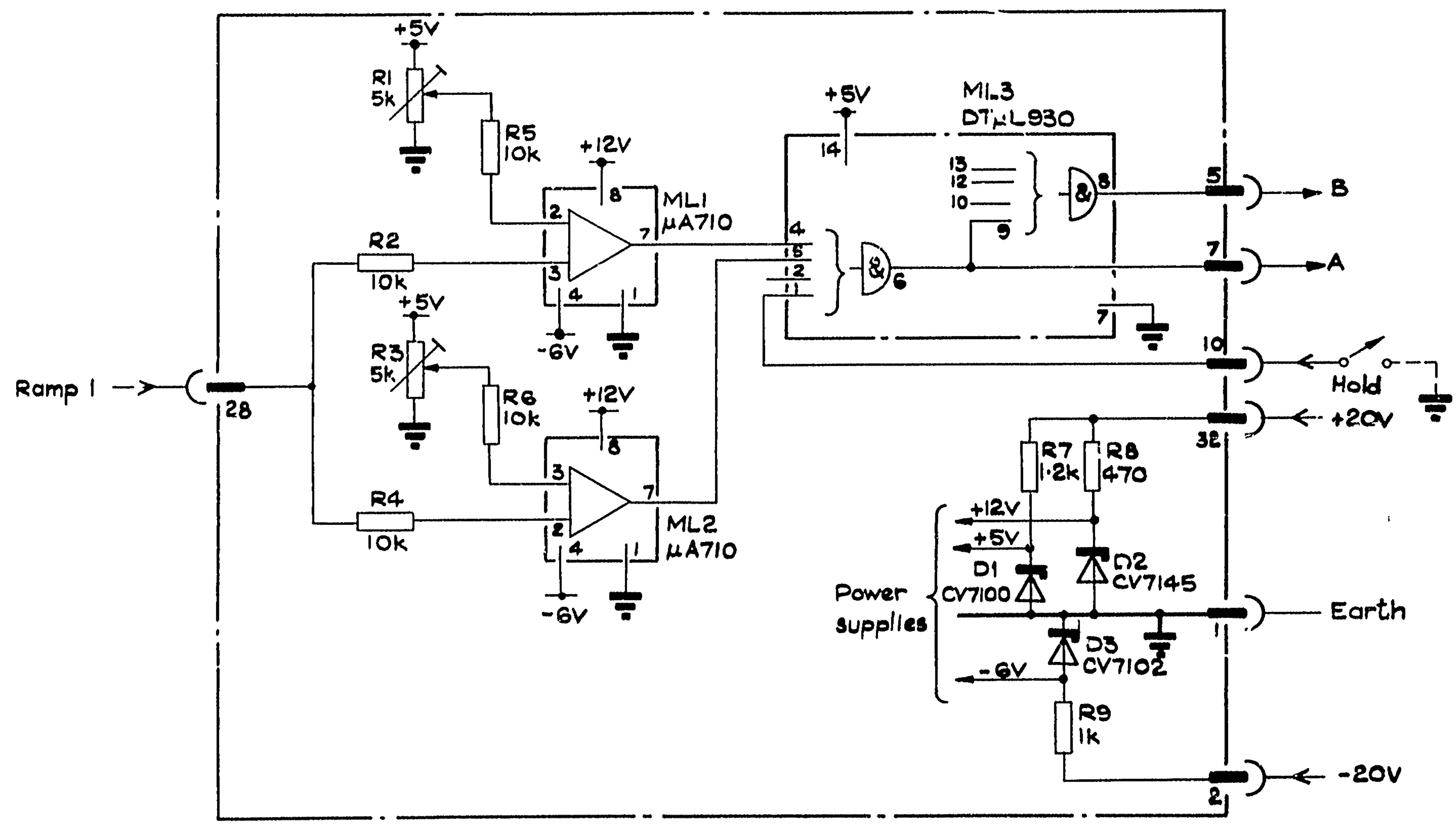

Fig.17 Range gate logic diagram

Fig. 17

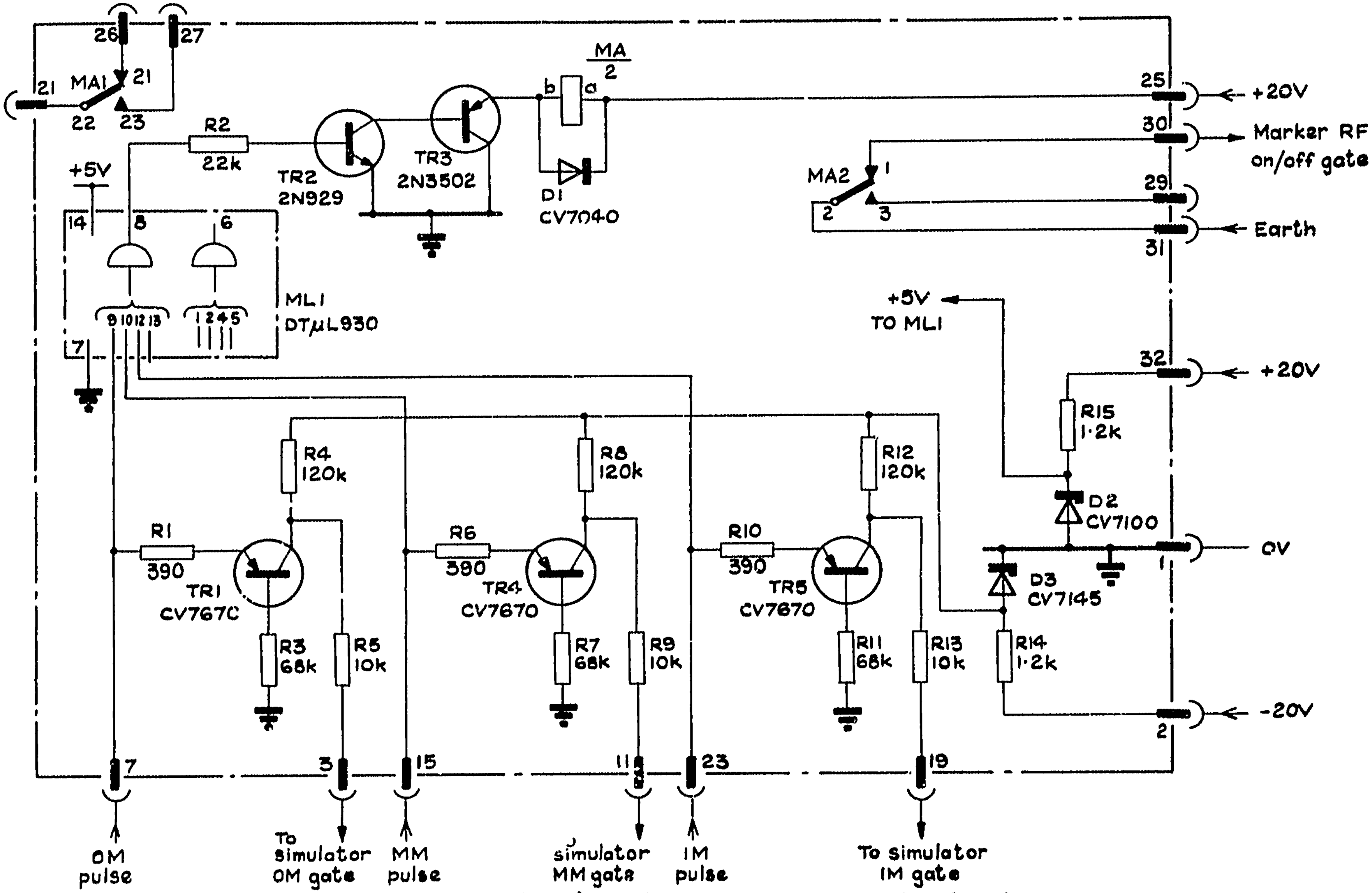

Fig. 18 Marker/simulator interface - circuit diagram

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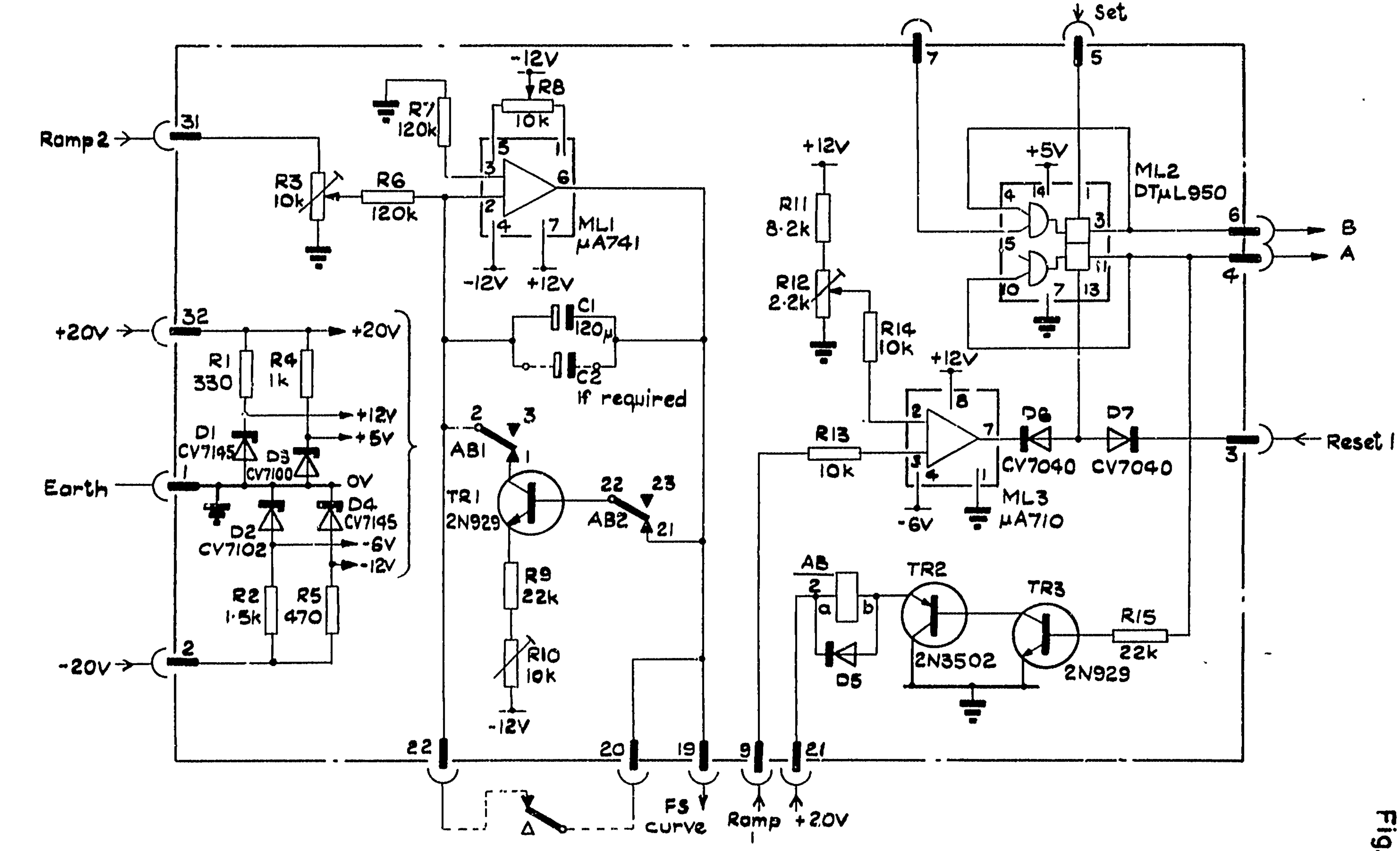

Fig. 19 Approach field strength curve generator-circuit diagram

Fig. 19

Fig. 20

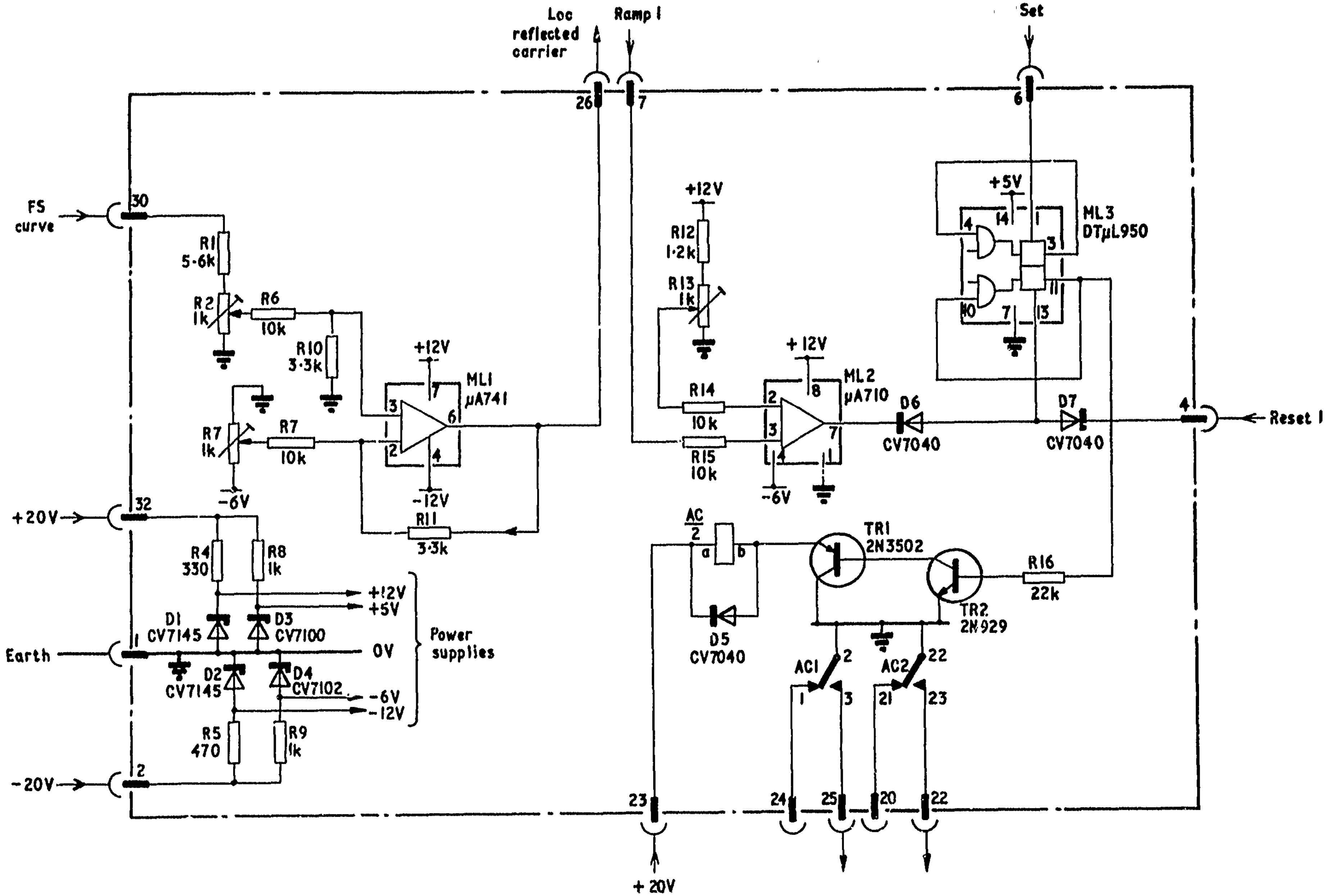

Fig. 20 Localiser field strength/simulator interface – circuit diagram

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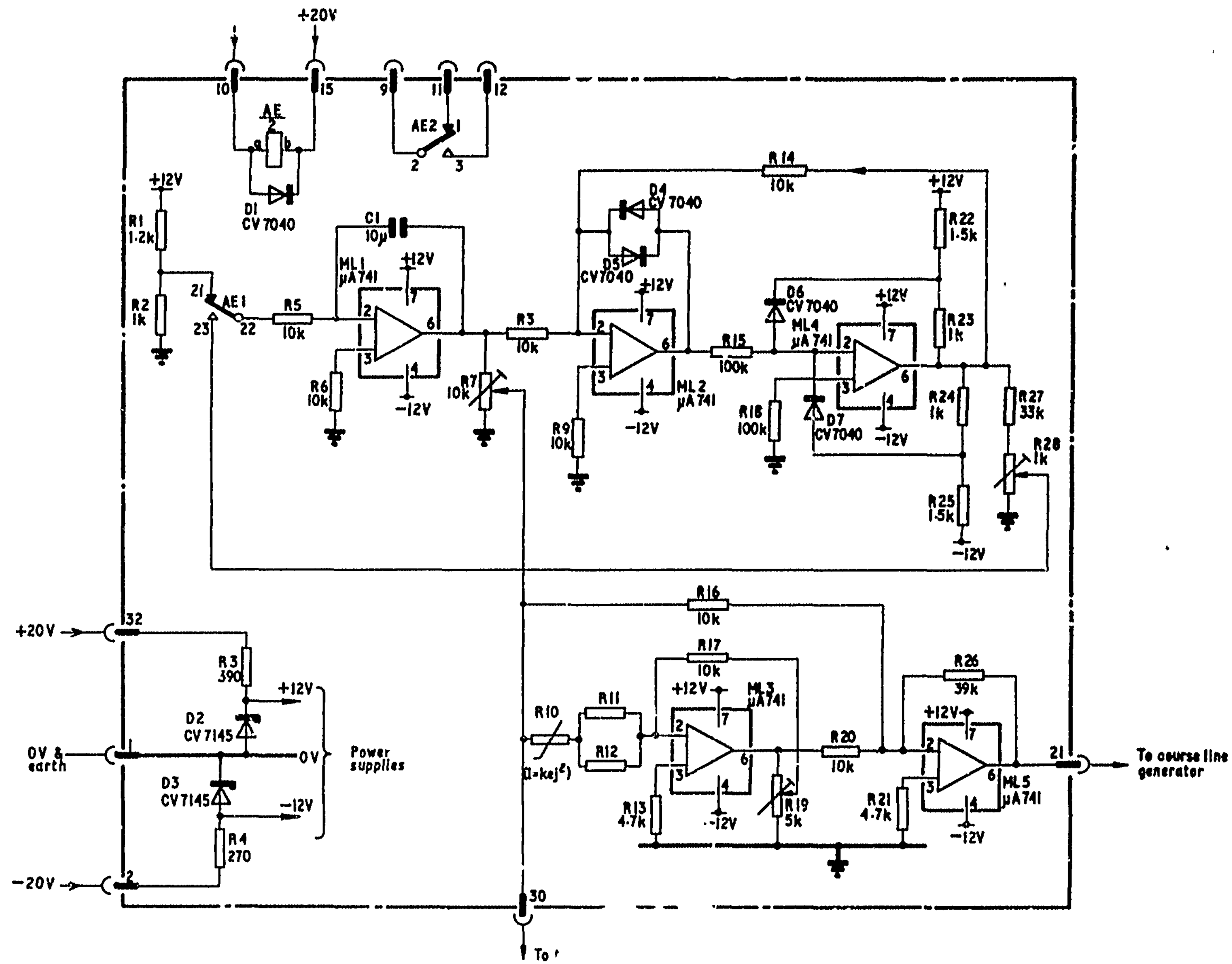

Fig.21 Sine waveform g... -circuit diagram

Fig.21

Fig.22 a-c

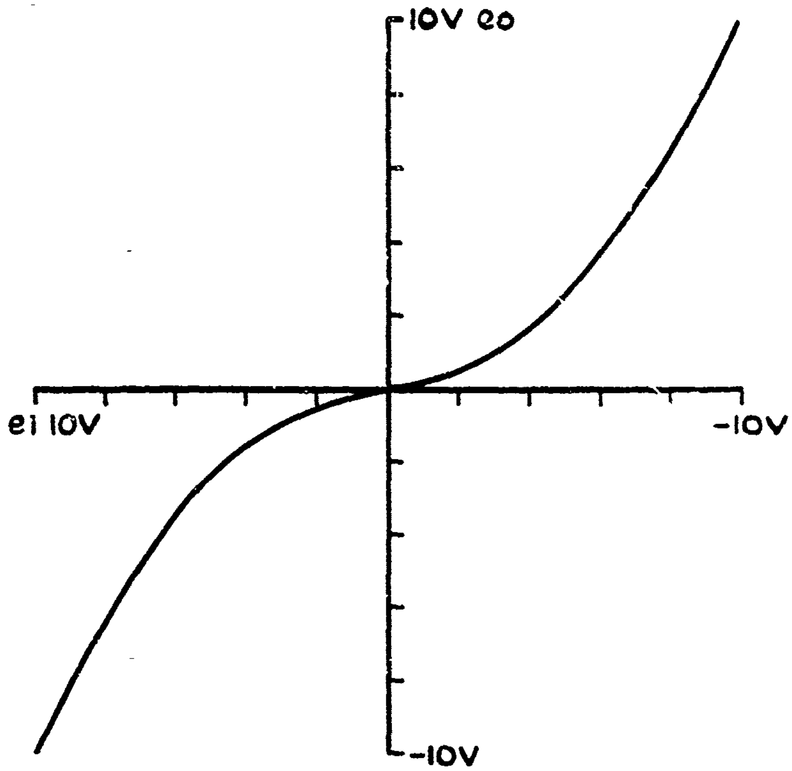

Fig.22a Output of ML 3

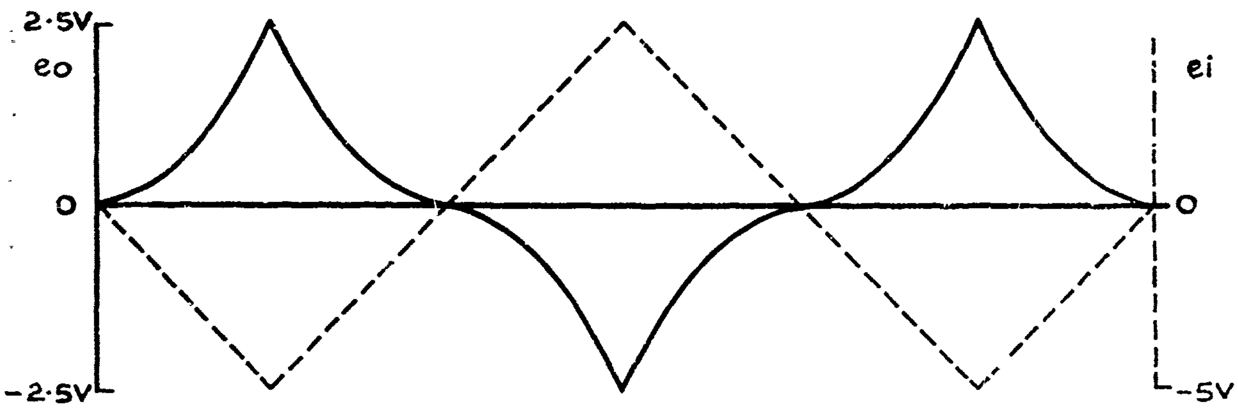

Fig.22b Inputs to ML 5

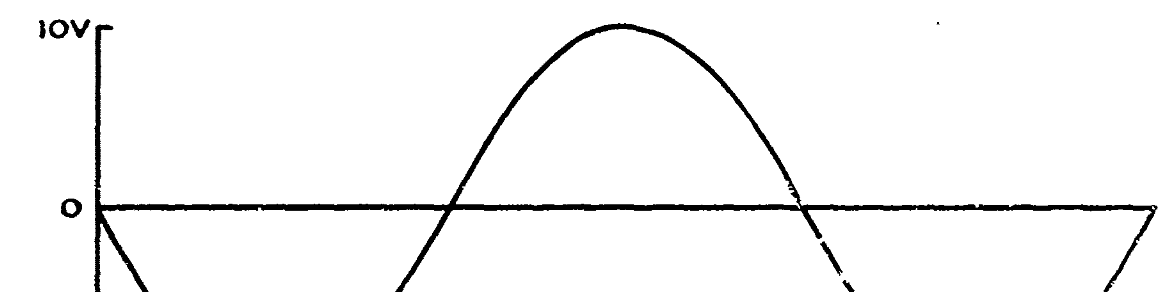

Fig.22c Output of ML5

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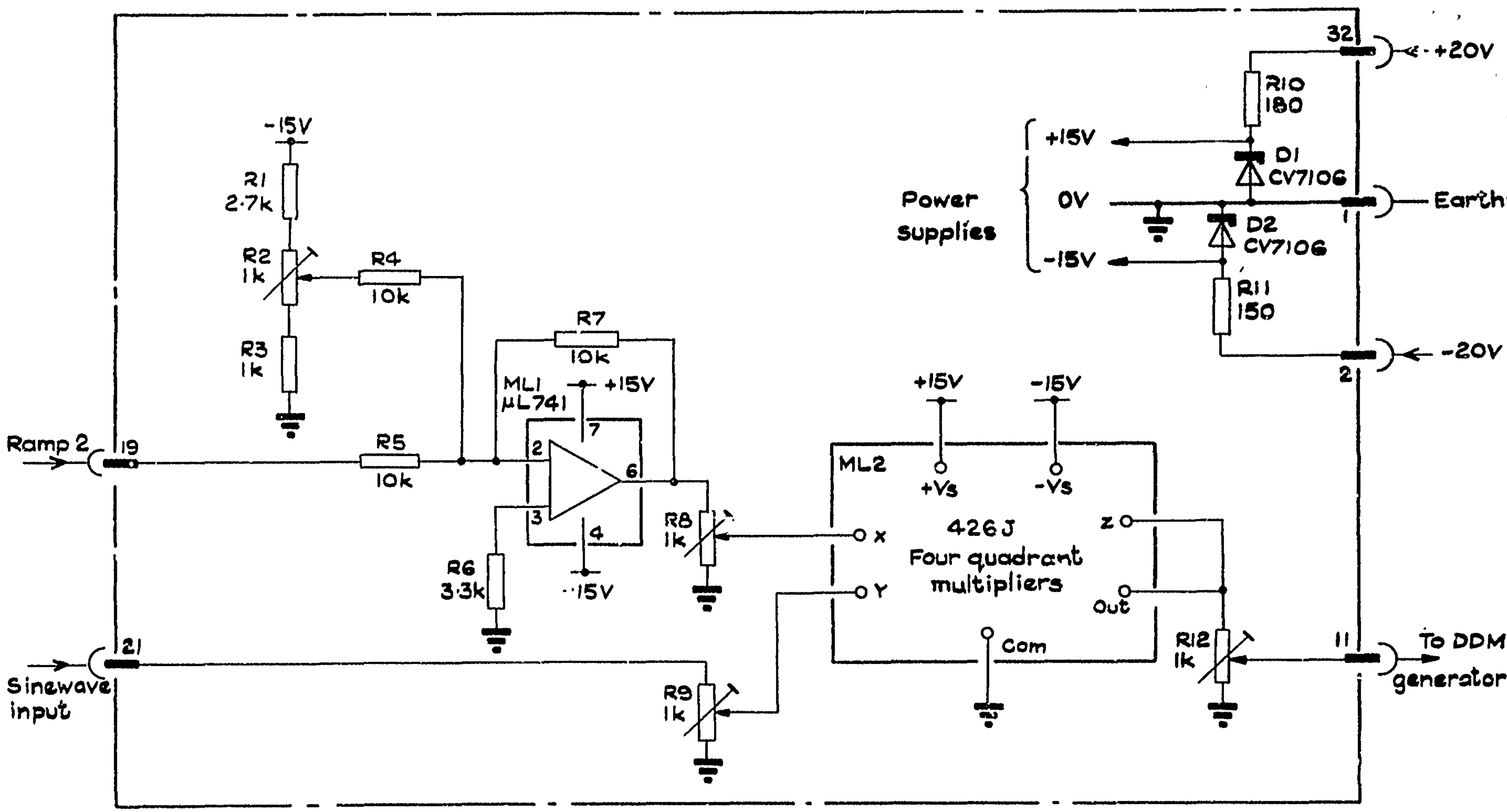

Fig. 23 Course line generator circuit diagram

Fig. 23

Fig. 24

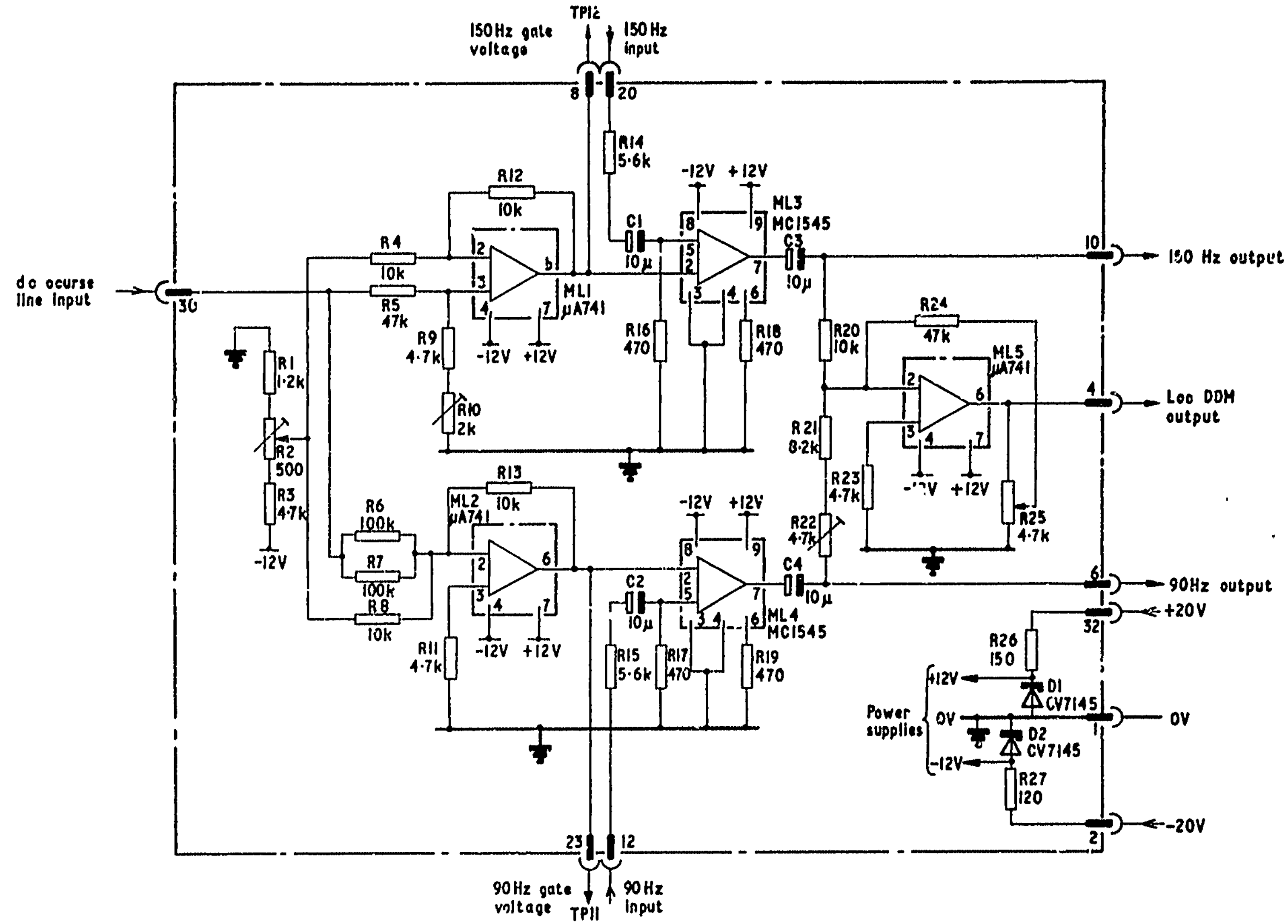

Fig. 24 Localiser DDM generator - circuit diagram

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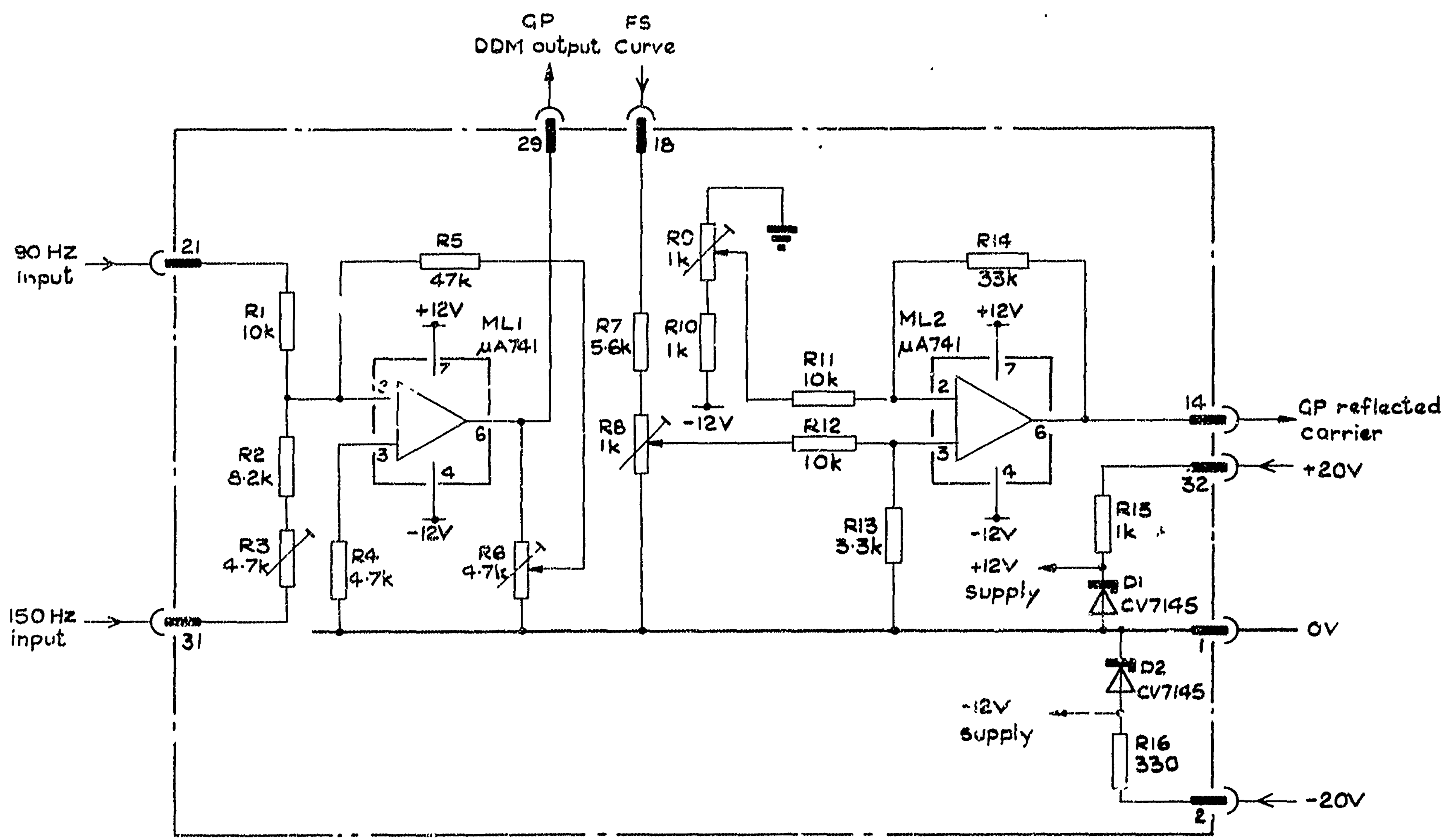

Fig. 25 Glide path reflected signal & DDM/simulator interface-circuit diagram

Fig. 25

Fig. 26

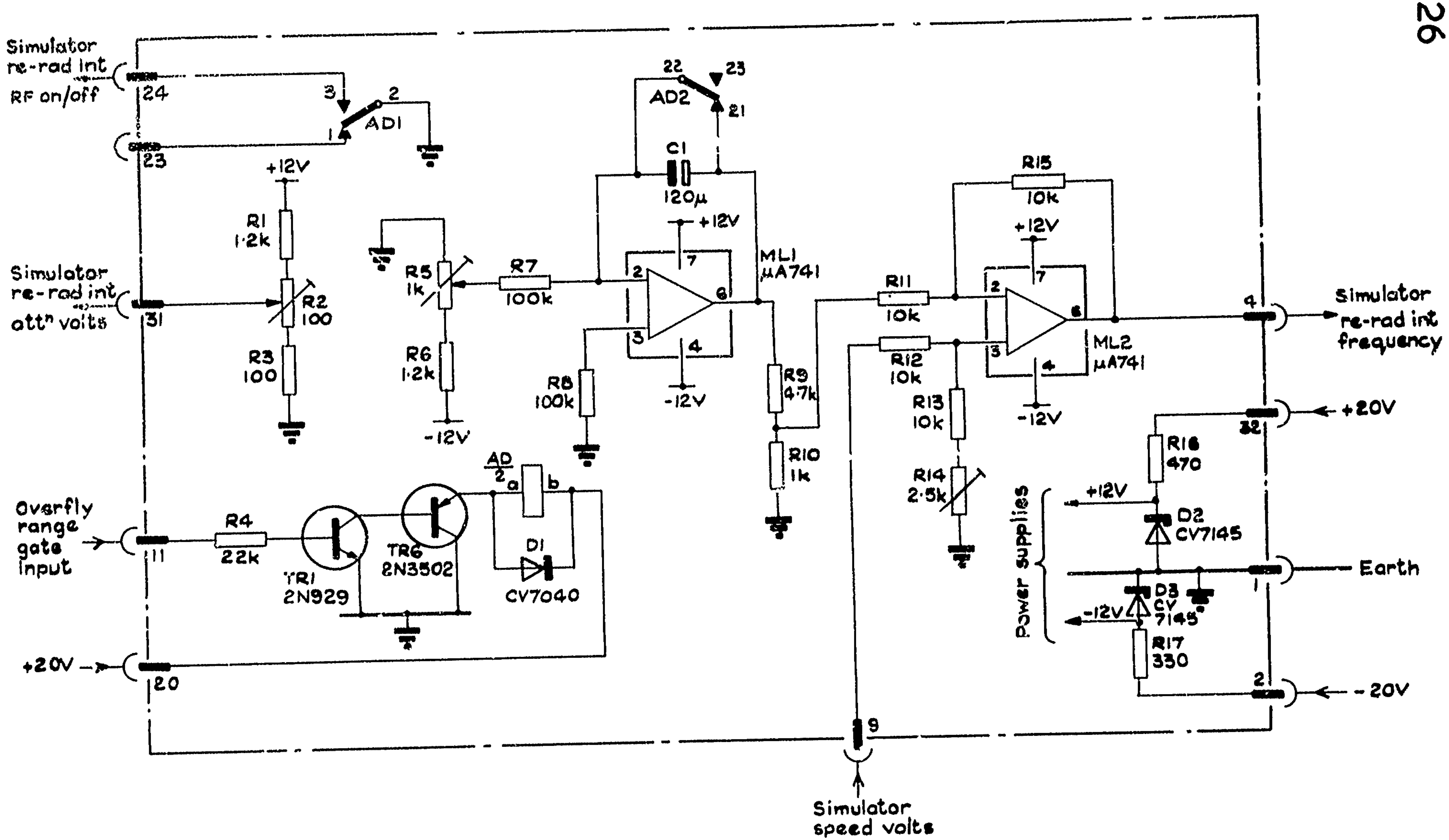

Fig. 26 Overfly interference gen & simulator interface-circuit diagram

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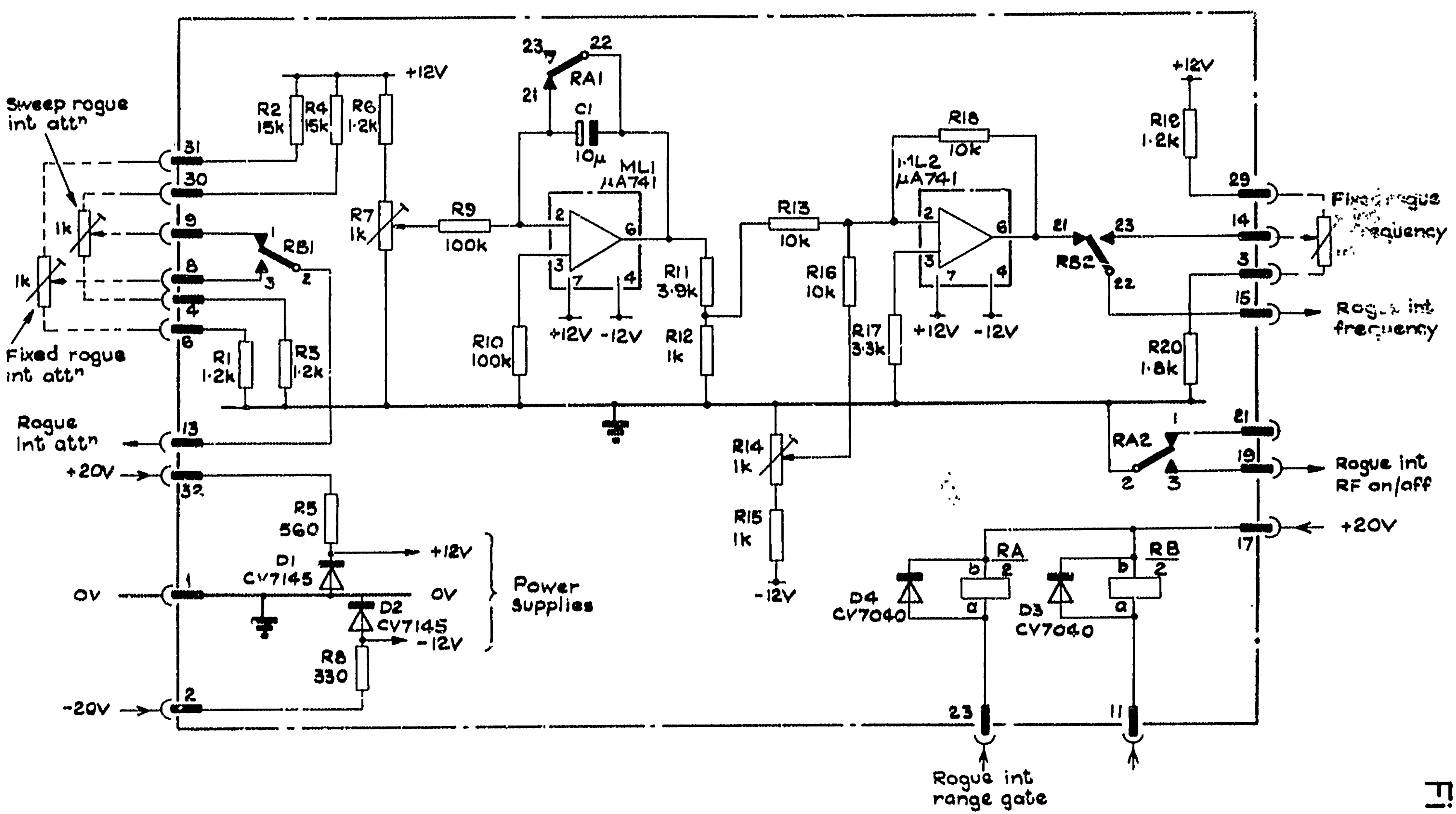

Fig. 27 GP-loc rogue interference generator & simulator interface-circuit diagram

Fig. 27

Fig. 28

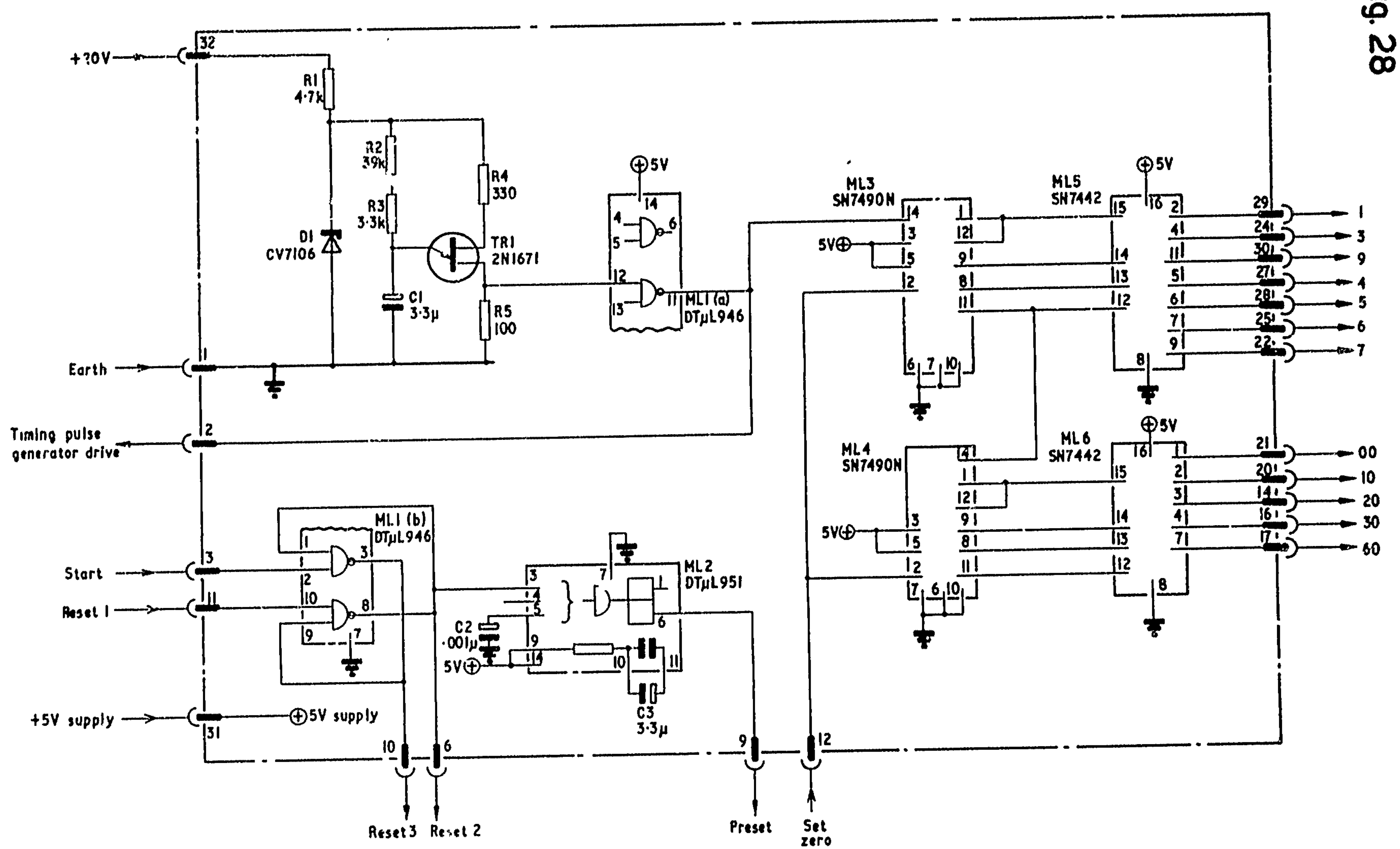

Fig. 28 Ident pulse gen-circuit diagram

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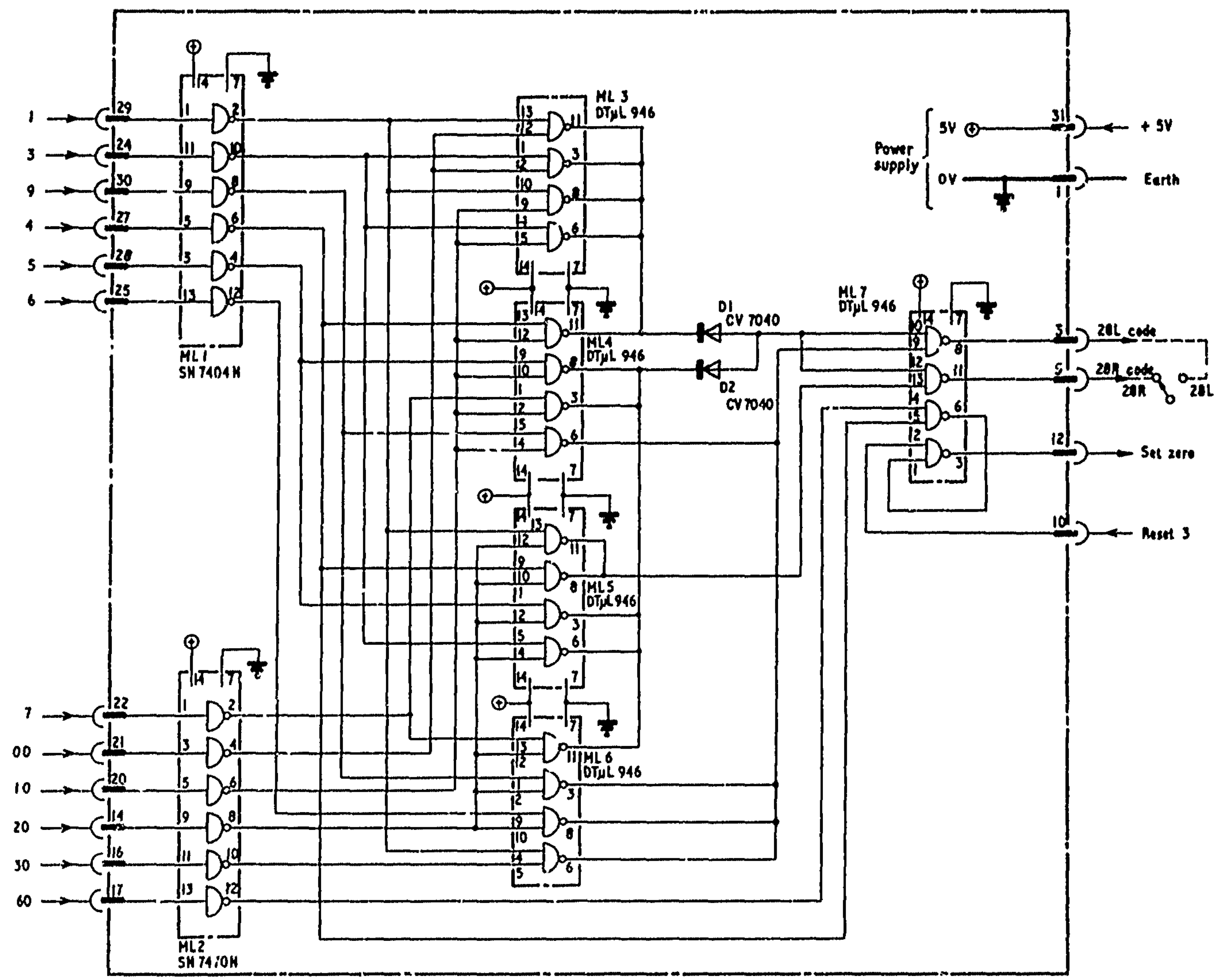

Fig. 29 Ident code gen-circuit diagram

Fig.29

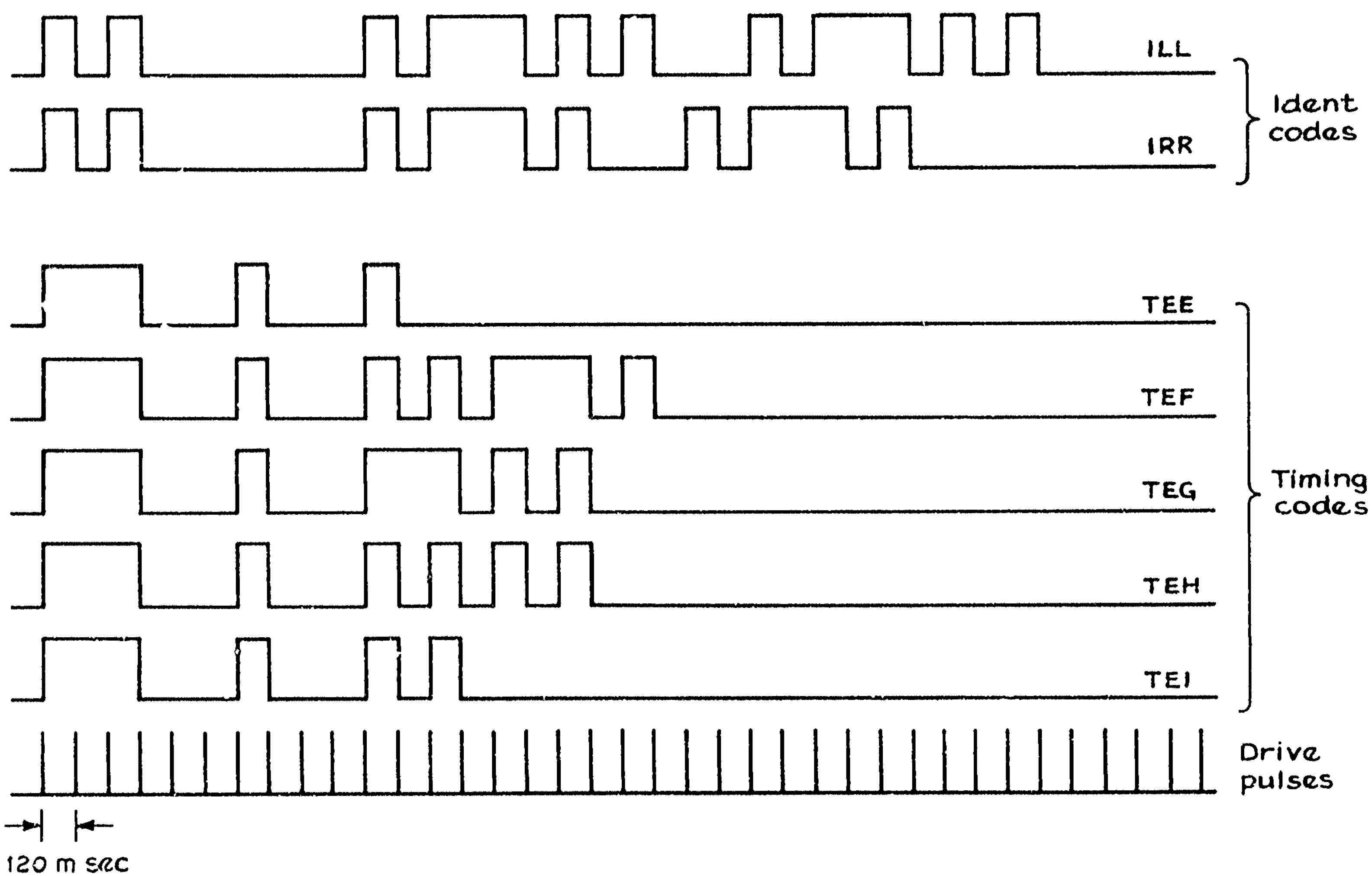

Fig. 30 Ident and timing codes

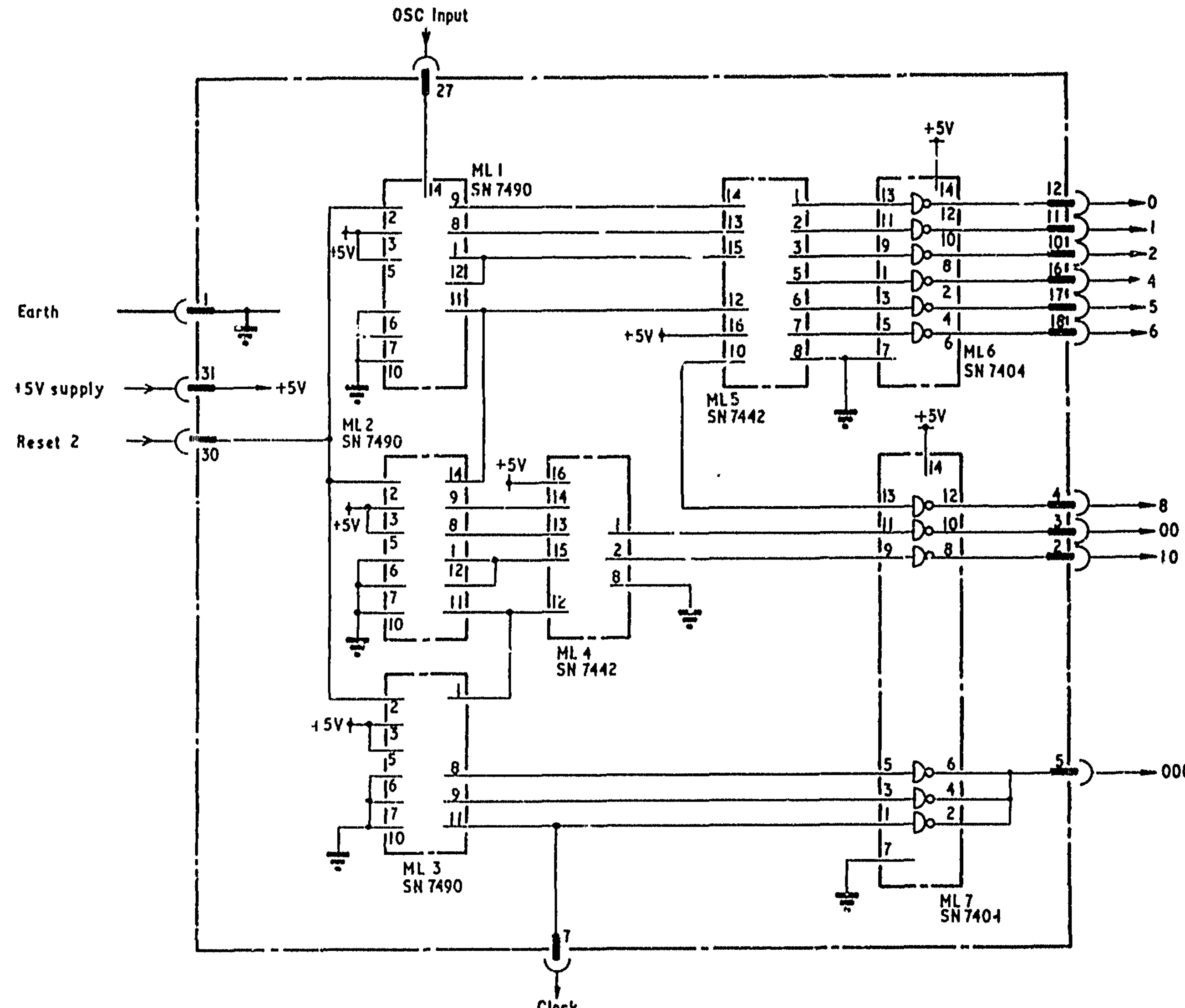

Fig. 31 Timing pulse generator-circuit diagram

Fig. 31

Fig. 32

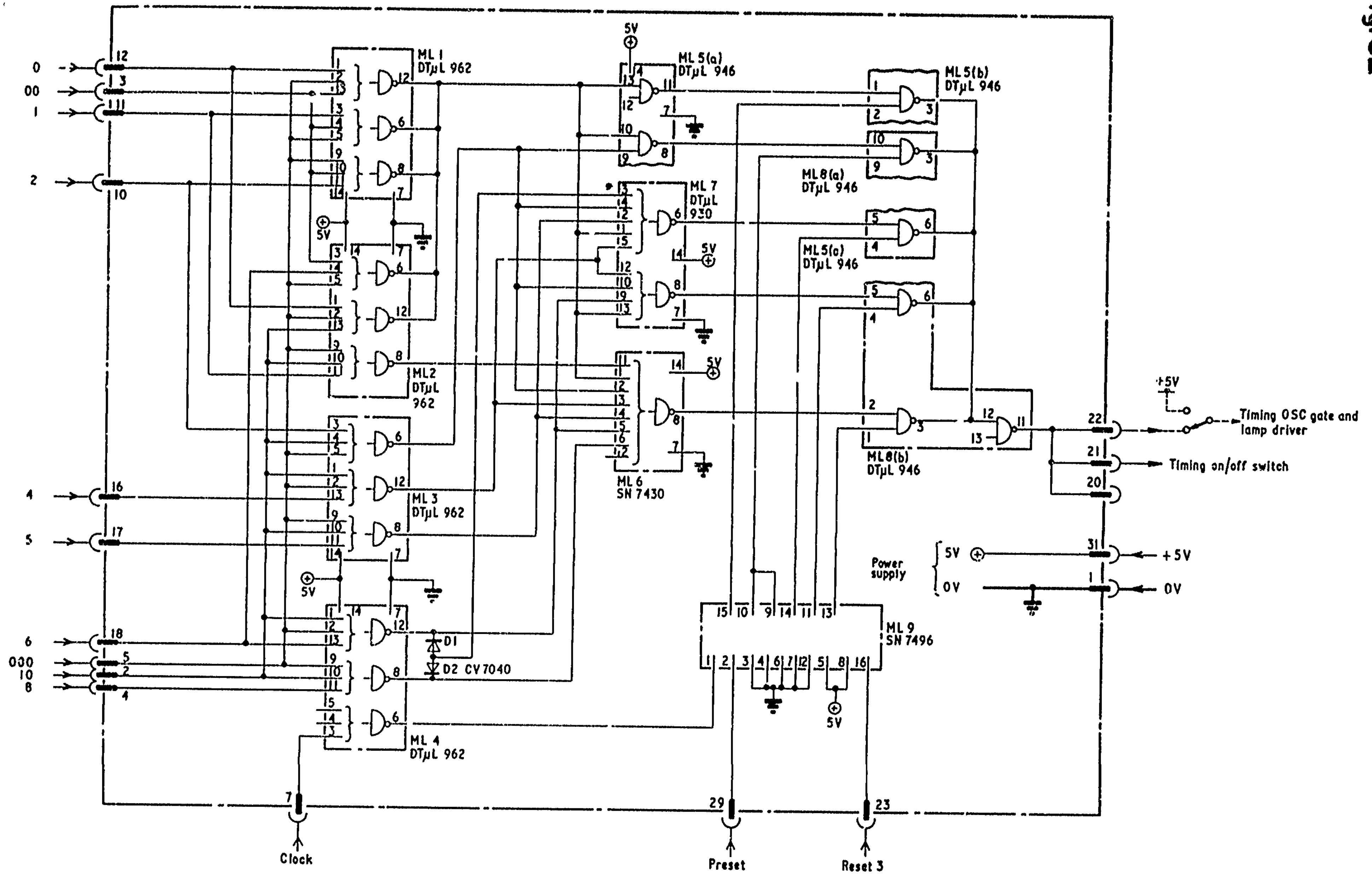

Fig. 32 Timing code generator-circuit diagram

904067

TR 71145

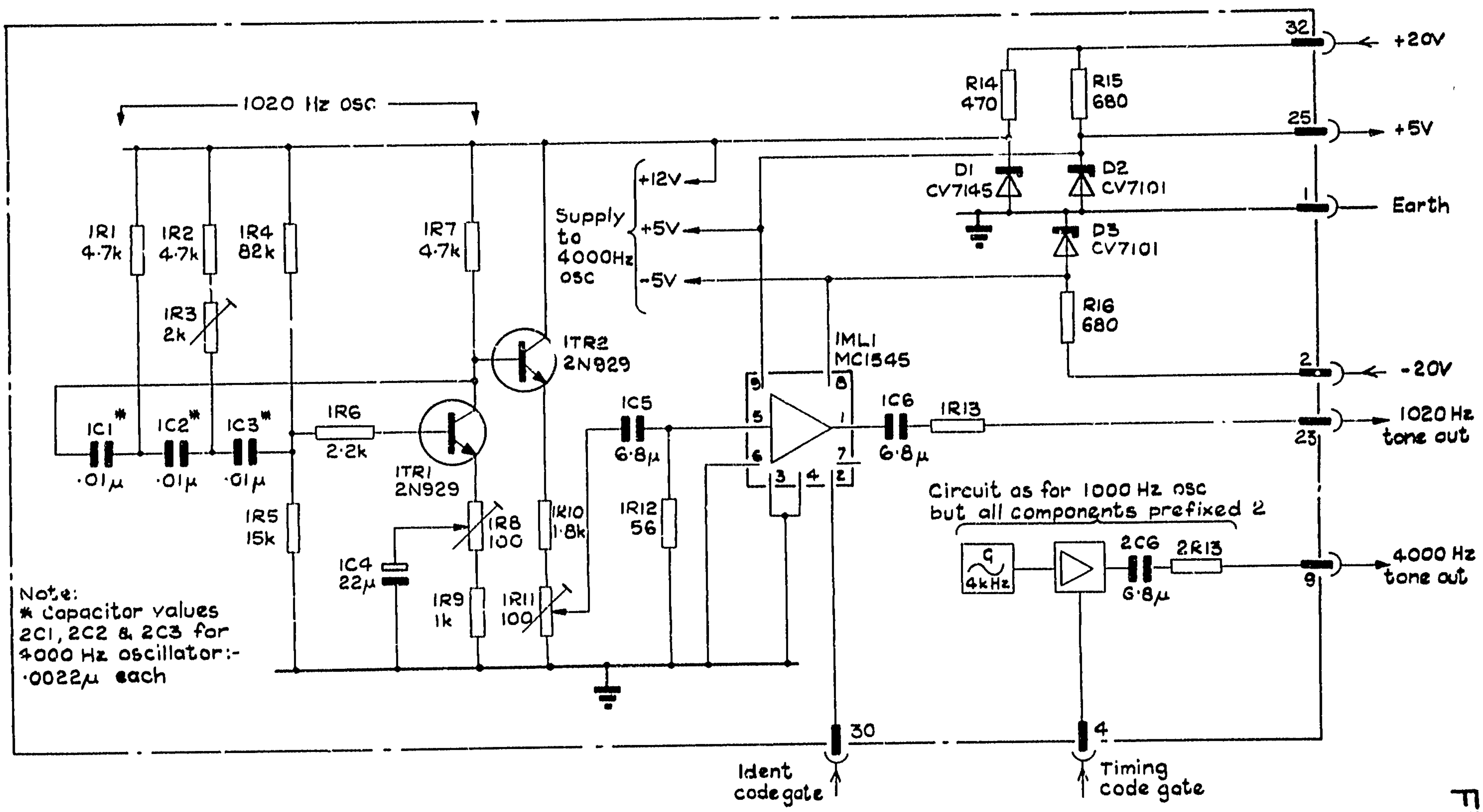

Fig. 33 1020/4000 Hz gated oscillator-circuit diagram

Fig. 33

Fig. 34

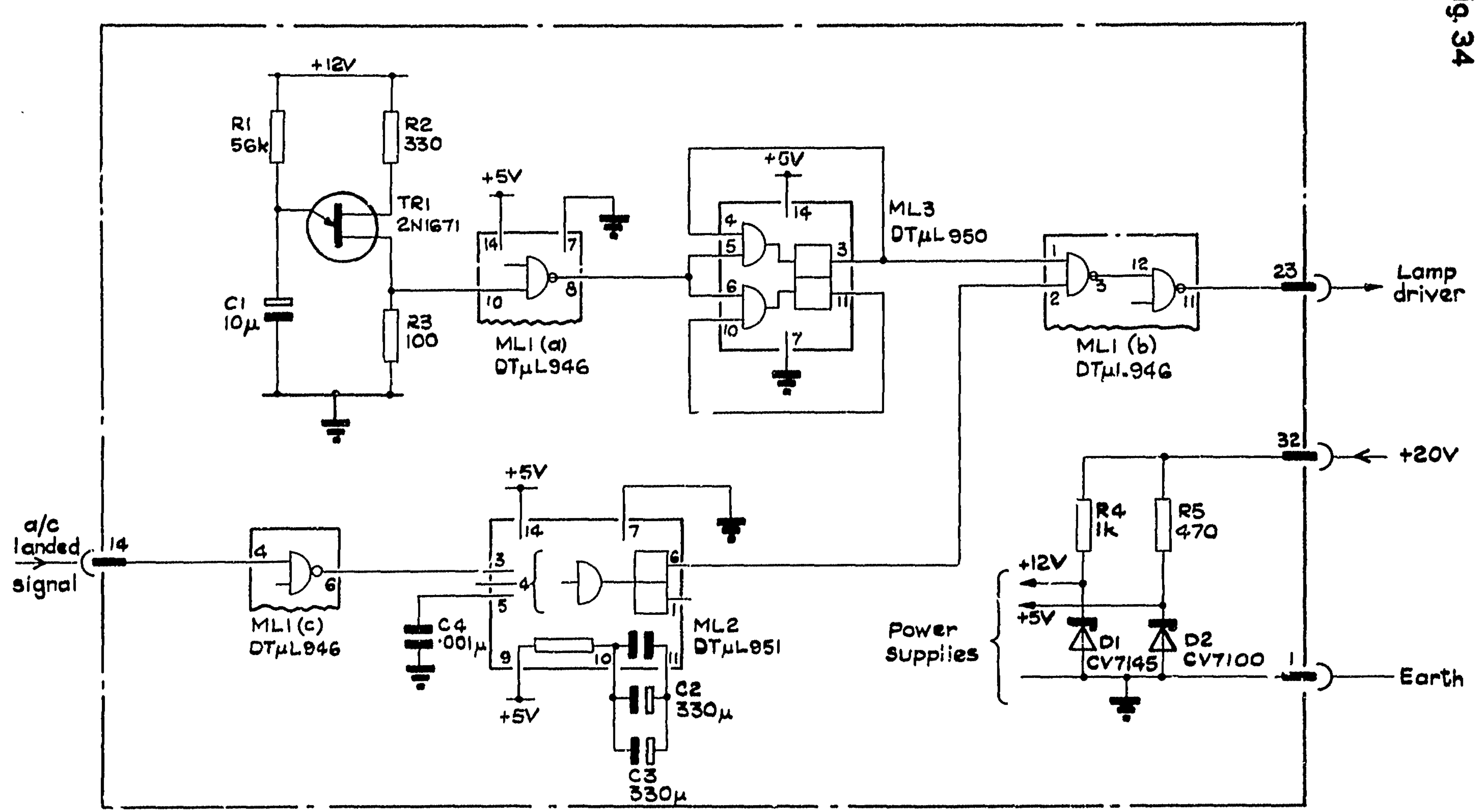

Fig. 34 Aircraft landed logic diagram

008 904069

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Fig.35

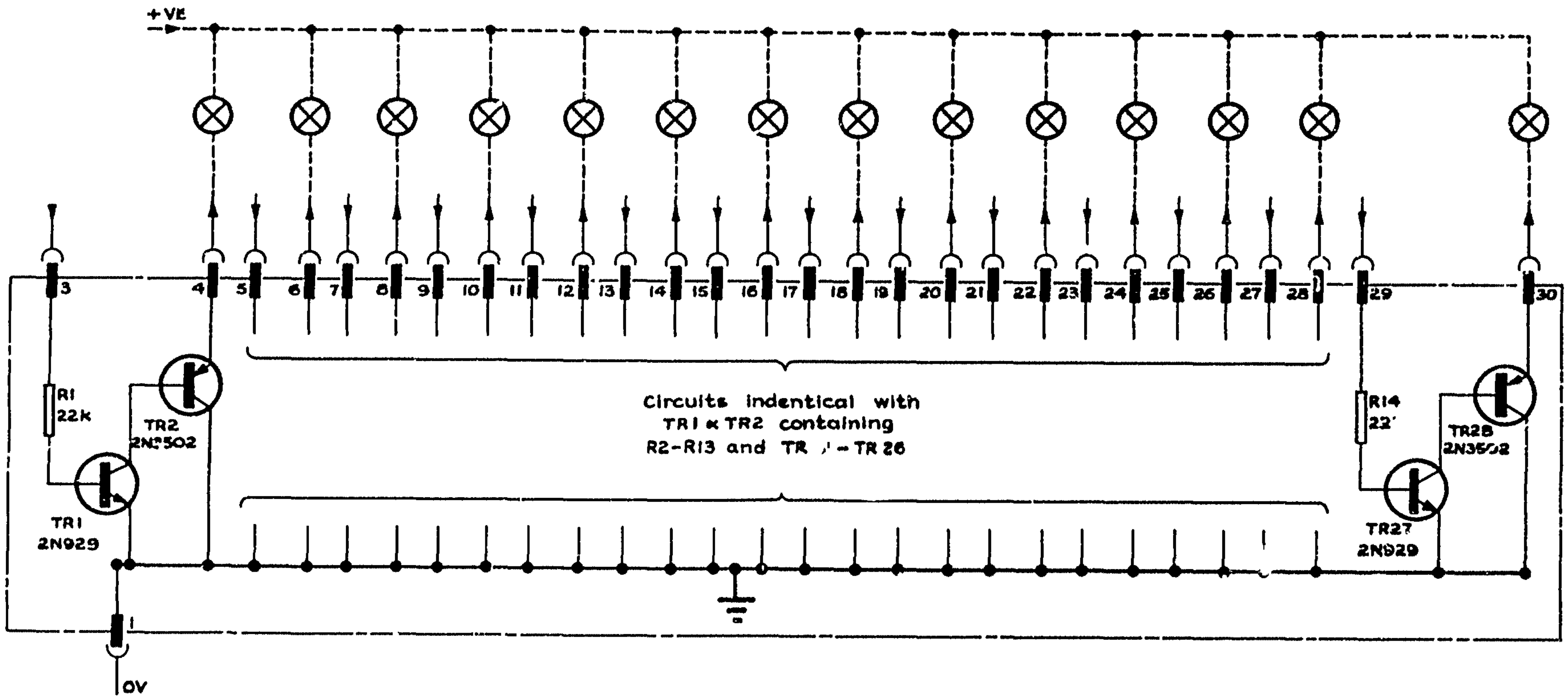

Fig.35 Lamp driver (14 stage) circuit diagram

Fig.36

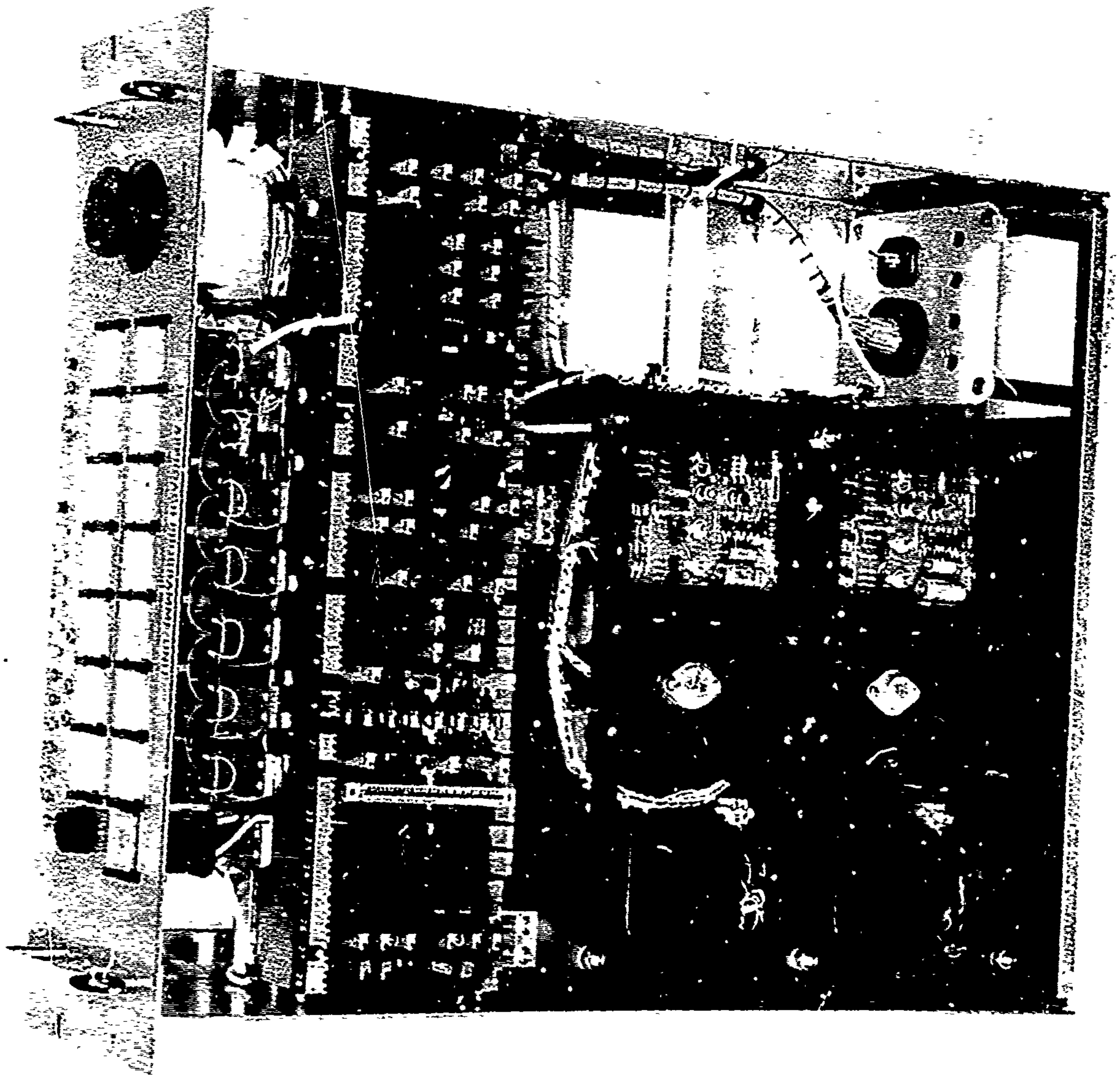

Fig.36. I.L.S. approach programme unit, top view

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